

N-Channel 100-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.024 at $V_{GS} = 10$ V	47
	0.027 at $V_{GS} = 4.5$ V	44

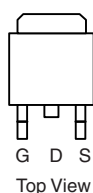
FEATURES

- TrenchFET® Power MOSFET
- 175 °C Maximum Junction Temperature
- 100 % R_g Tested

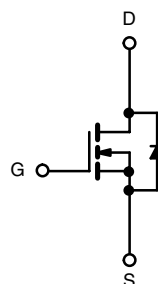


RoHS
COMPLIANT

TO-263



Ordering Information: SUM47N10-24L-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C) ^b	I_D	47	A
		27	
Pulsed Drain Current	I_{DM}	70	
Continuous Source Current (Diode Conduction)	I_S	47	
Single Pulse Avalanche Current	I_{AS}	40	mJ
Single Pulse Avalanche Energy (Duty Cycle ≤ 1 %)	E_{AS}	80	
Maximum Power Dissipation	P_D	136 ^b	W
		3.75 ^a	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Unit
Junction-to-Ambient	R_{thJA}	40	°C/W
		62.5	
Junction-to-Case	R_{thJC}	1.1	

Notes:

a. Surface Mounted on 1" x 1" FR4 Board.

b. See SOA curve for voltage derating.

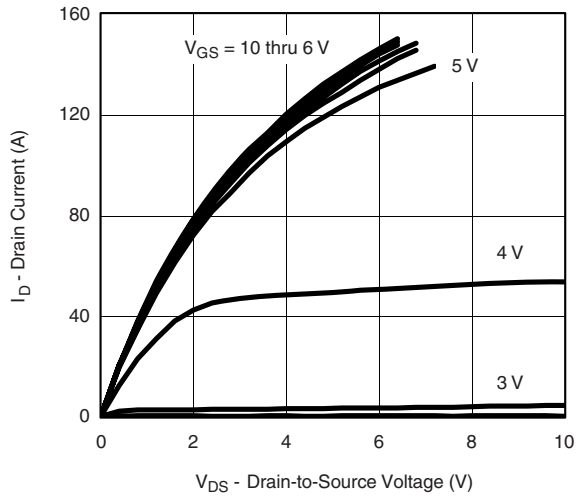
SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	100			V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 175 °C			250	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	70			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 40 A		0.019	0.024	Ω
		V _{GS} = 10 V, I _D = 40 A, T _J = 125 °C			0.048	
		V _{GS} = 10 V, I _D = 40 A, T _J = 175 °C			0.060	
		V _{GS} = 4.5 V, I _D = 20 A		0.021	0.027	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 40 A		70		S
Dynamic ^a						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, F = 1 MHz		2400		pF
Output Capacitance	C _{oss}			290		
Reverse Transfer Capacitance	C _{rss}			120		
Total Gate Charge ^c	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 40 A		40	60	nC
Gate-Source Charge ^c	Q _{gs}			11		
Gate-Drain Charge ^c	Q _{gd}			9		
Gate Resistance	R _g	f = 1 MHz	1	2.2	3.5	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 50 V, R _L = 1.25 Ω I _D ≅ 47 A, V _{GEN} = 10 V, R _g = 2.5 Ω		8	13	ns
Rise Time ^c	t _r			40	60	
Turn-Off Delay Time ^c	t _{d(off)}			15	25	
Fall Time ^c	t _f			80	120	
Source-Drain Diode Ratings and Characteristics T _C = 25 °C						
Pulsed Current	I _{SM}				70	A
Diode Forward Voltage ^b	V _{SD}	I _F = 40 A, V _{GS} = 0 V		1.0	1.5	V
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 47 A, di/dt = 100 A/μs		75	120	ns

Notes:

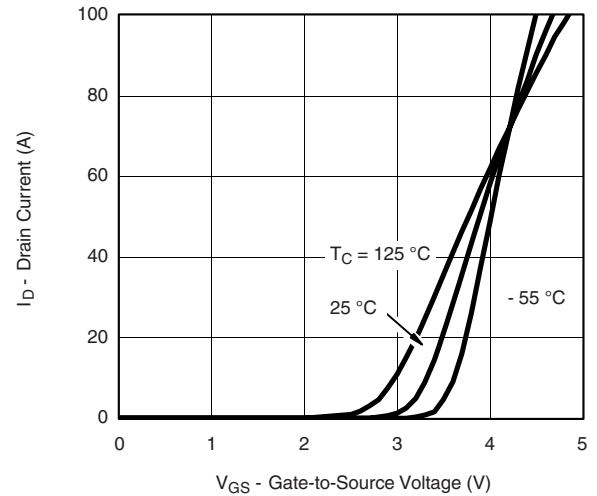
- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

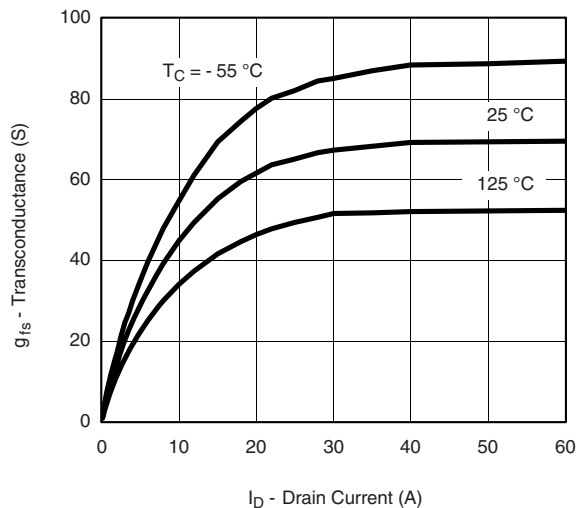
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



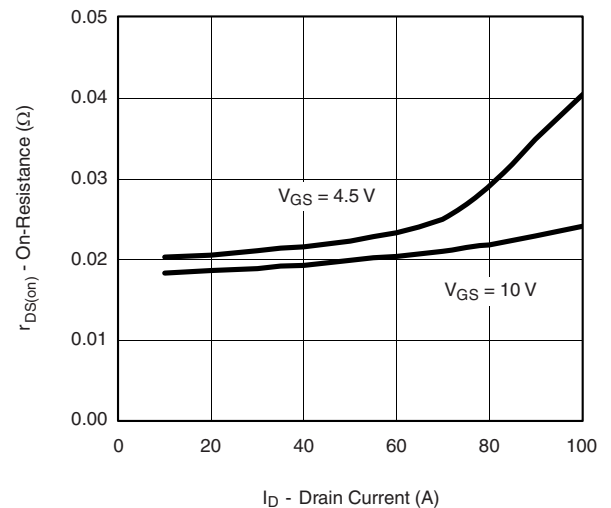
Output Characteristics



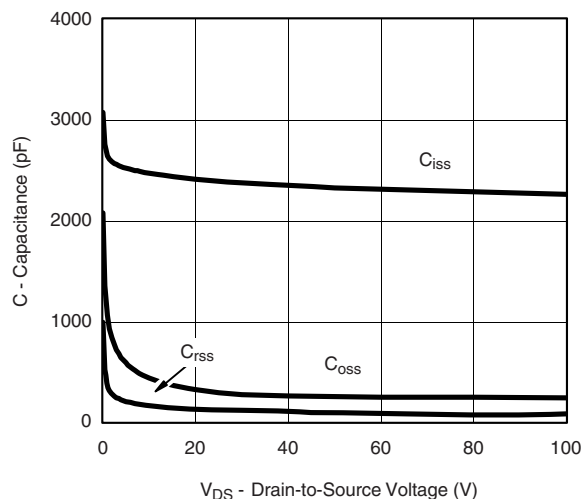
Transfer Characteristics



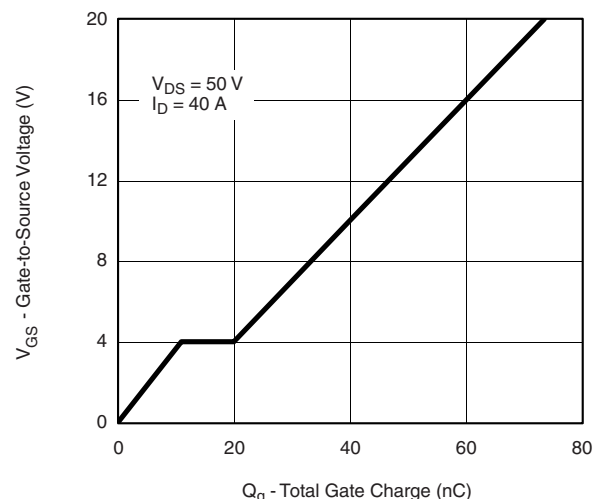
Transconductance



On-Resistance vs. Drain Current

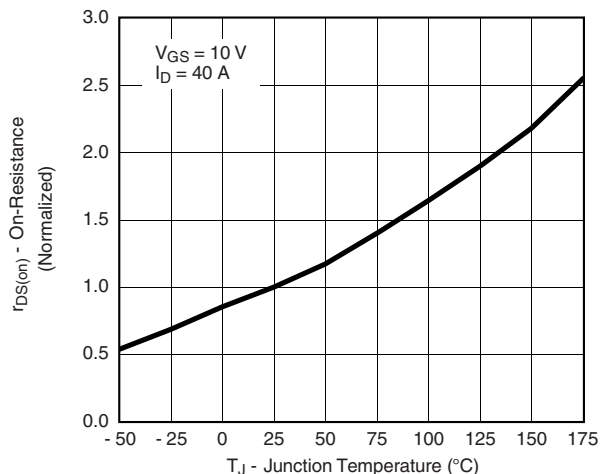


Capacitance

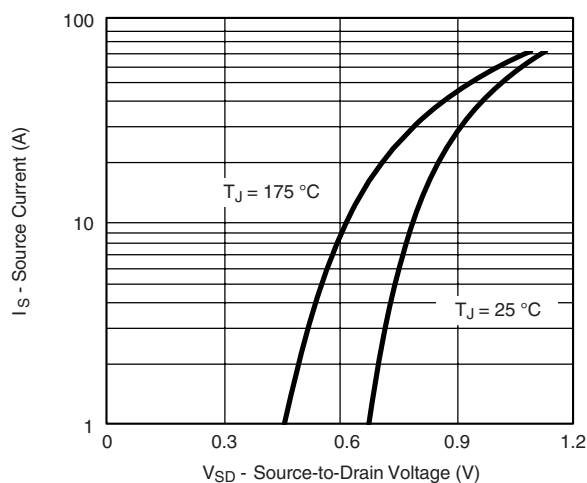


Gate Charge

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

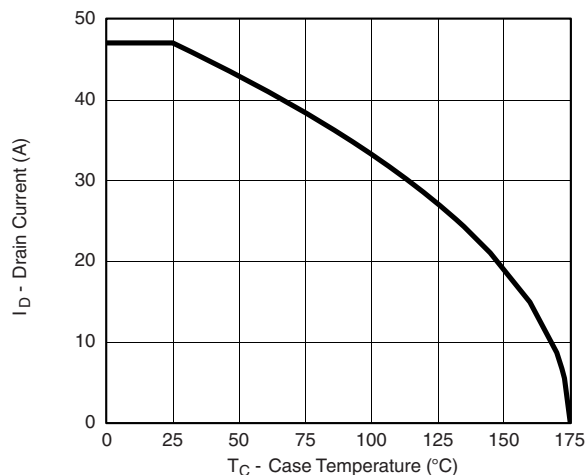


On-Resistance vs. Junction Temperature

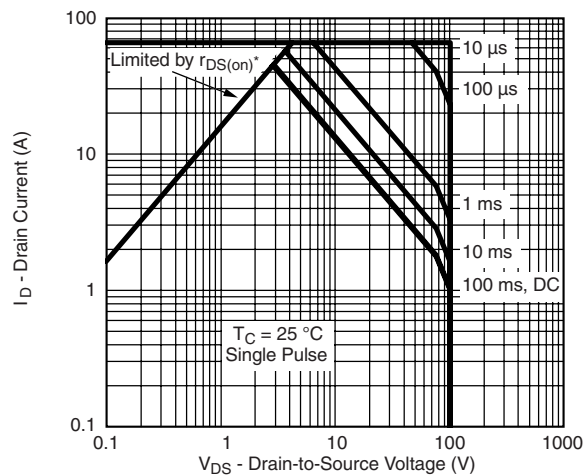


Source-Drain Diode Forward Voltage

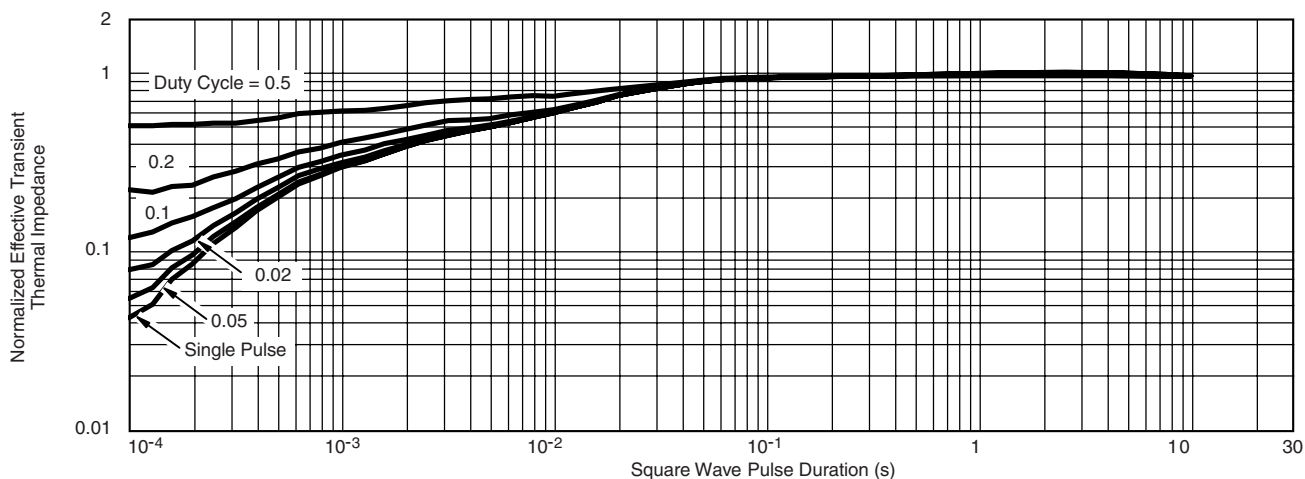
THERMAL RATINGS



Maximum Avalanche Drain Current vs. Case Temperature



* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

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