

N-Channel 1.2 V (G-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
8	0.031 at V _{GS} = 4.5 V	12.2	20 nC
	0.033 at V _{GS} = 2.5 V	11.6	
	0.035 at V _{GS} = 1.8 V	11.2	
	0.043 at V _{GS} = 1.5 V	10.2	
	0.077 at V _{GS} = 1.2 V	1.3	

FEATURES

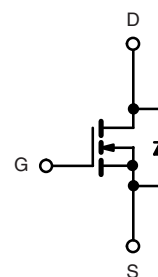
- TrenchFET[®] Power MOSFET
- Industry First 1.2 V Rated MOSFET
- Ultra Small MICRO FOOT[®] ChipScale Packaging Reduces Footprint Area, Profile (0.62 mm) and On-Resistance Per Footprint Area
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



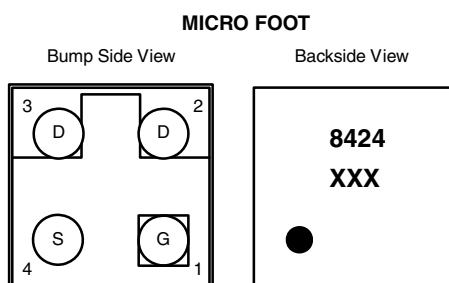
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Low Threshold Load Switch for Portable Devices
 - Low Power Consumption
 - Increased Battery Life
- Ultra Low Voltage Load Switch



N-Channel MOSFET



Device Marking: 8424
xxx = Date/Lot Traceability Code

Ordering Information: Si8424DB-T1-E1 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	8	V
Gate-Source Voltage		V _{GS}	± 5	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	12.2	A
	T _C = 70 °C		9.8	
	T _A = 25 °C		8.1 ^{b,c}	
	T _A = 70 °C		6.5 ^{b,c}	
Pulsed Drain Current		I _{DM}	20	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	5.2	
	T _A = 25 °C		2.3 ^{b,c}	
Maximum Power Dissipation	T _C = 25 °C	P _D	6.25	W
	T _C = 70 °C		4	
	T _A = 25 °C		2.78 ^{b,c}	
	T _A = 70 °C		1.78 ^{b,c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C
Package Reflow Conditions ^d		IR/Convection	260	

Notes:

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
- In this document, any reference to the Case represents the body of the MICRO FOOT device and Foot is the bump.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typ.	Max.	Unit
Maximum Junction-to-Ambient ^{a,b}	R_{thJA}	35	45	°C/W
Maximum Junction-to-Foot (Drain)	Steady State R_{thJF}	16	20	

Notes

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under steady state conditions is 72 °C/W.

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	8			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		8.9		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 2.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.35		1	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 5\text{ V}$			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 8\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 8\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ °C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 5\text{ V}, V_{GS} = 4.5\text{ V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 1\text{ A}$		0.025	0.031	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 1\text{ A}$		0.027	0.033	
		$V_{GS} = 1.8\text{ V}, I_D = 1\text{ A}$		0.029	0.035	
		$V_{GS} = 1.5\text{ V}, I_D = 1\text{ A}$		0.032	0.043	
		$V_{GS} = 1.2\text{ V}, I_D = 1\text{ A}$		0.049	0.077	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 4\text{ V}, I_D = 1\text{ A}$		8.3	13	S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 4\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1950		pF
Output Capacitance	C_{oss}			610		
Reverse Transfer Capacitance	C_{rss}			350		
Total Gate Charge	Q_g	$V_{DS} = 4\text{ V}, V_{GS} = 5\text{ V}, I_D = 1\text{ A}$		22	33	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 4\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 1\text{ A}$		20	30	
Gate-Drain Charge	Q_{gd}			3.5		
Gate Resistance	R_g			1.8		
Gate Resistance	R_g	$V_{GS} = 0.1\text{ V}, f = 1\text{ MHz}$		13		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 4\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		8	12	ns
Rise Time	t_r			12	18	
Turn-Off Delay Time	$t_{d(off)}$			110	165	
Fall Time	t_f			40	60	

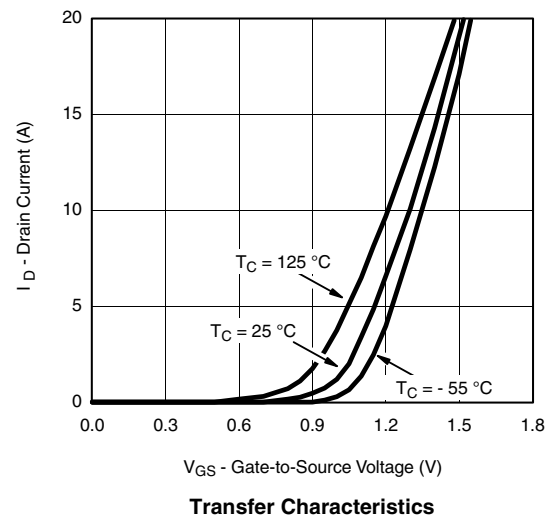
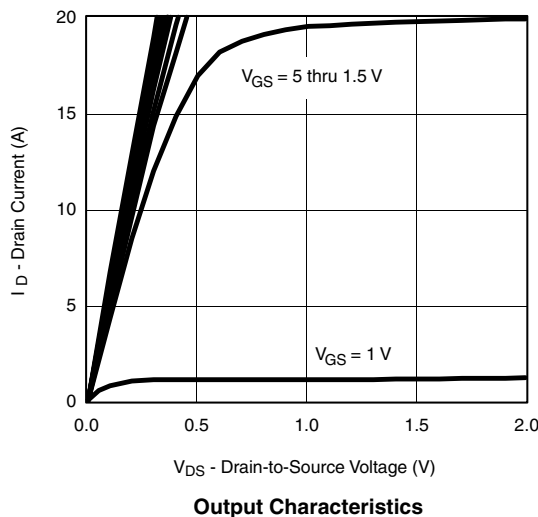
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			6.25	A
Pulse Diode Forward Current	I_{SM}				20	
Body Diode Voltage	V_{SD}	$I_S = 1\text{ A}, V_{GS} = 0\text{ V}$		0.6	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		104	156	ns
Body Diode Reverse Recovery Charge	Q_{rr}			88	132	nC
Reverse Recovery Fall Time	t_a			26		ns
Reverse Recovery Rise Time	t_b			78		

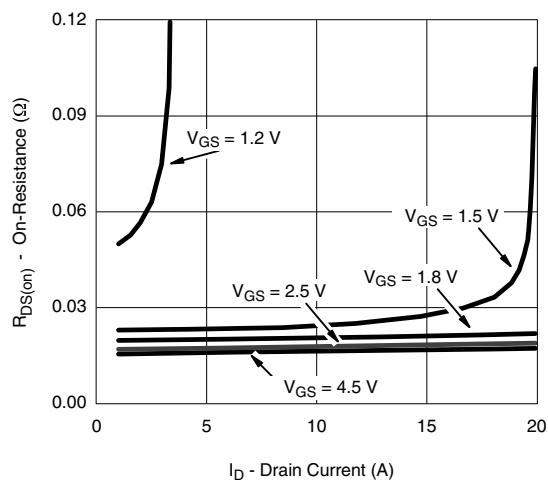
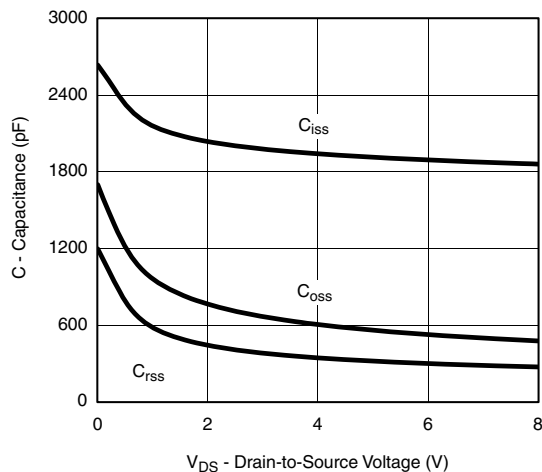
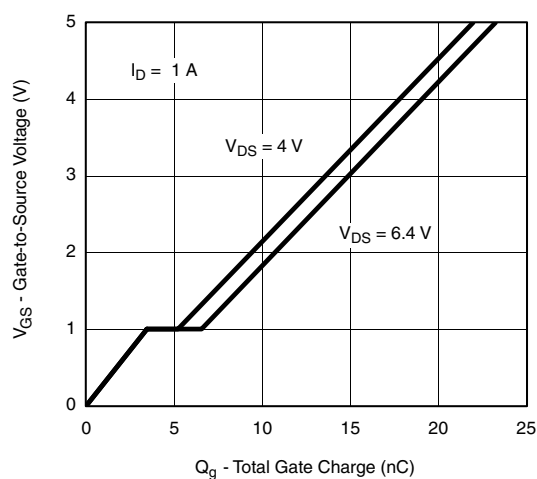
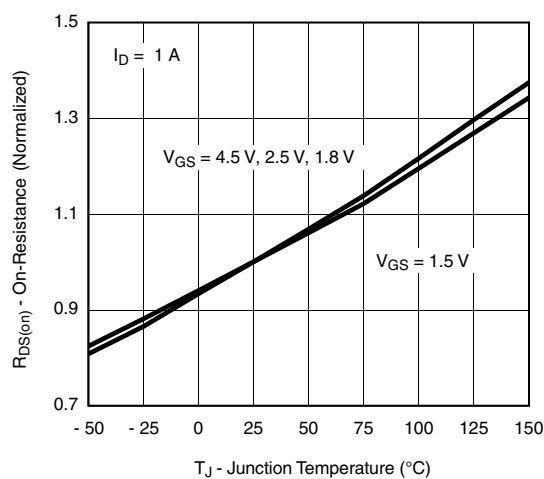
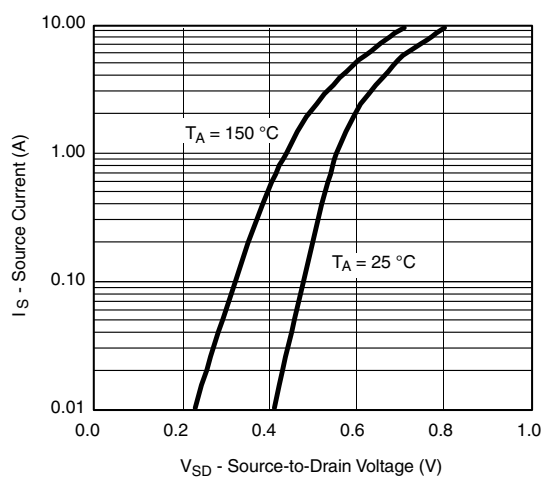
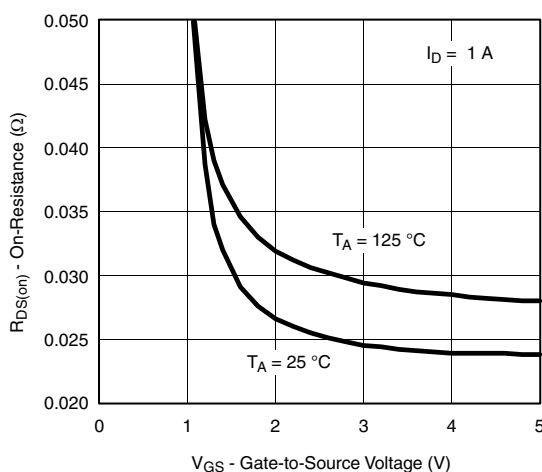
Notes:

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

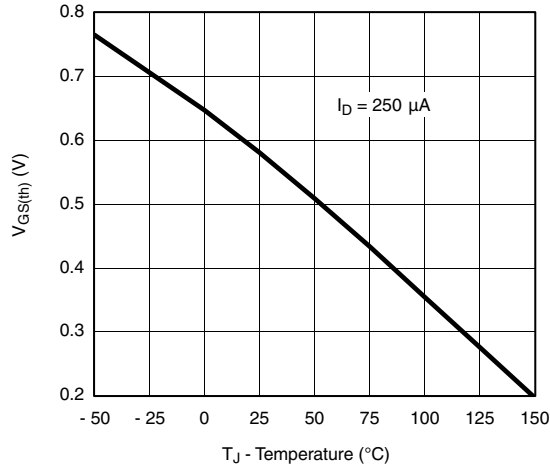
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

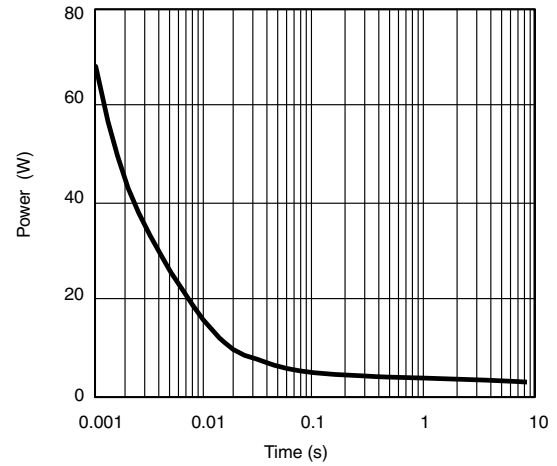


TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

 $R_{DS(on)}$ vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

Forward Diode Voltage vs Temp

 $R_{DS(on)}$ vs V_{GS} vs Temperature

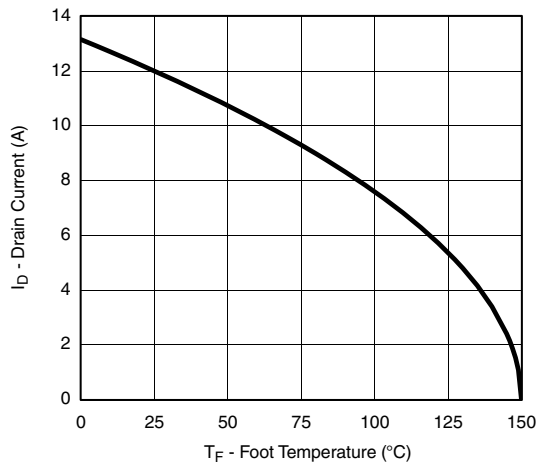
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



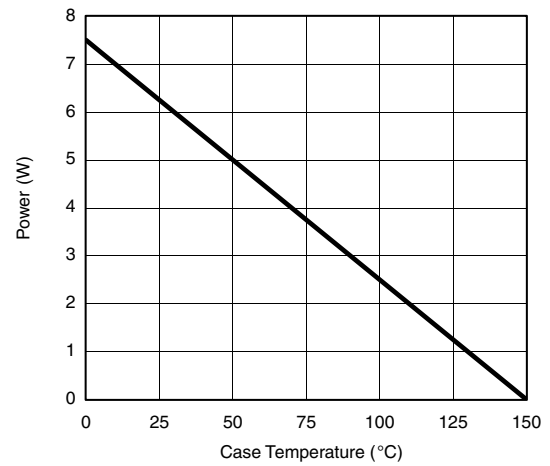
Threshold Voltage



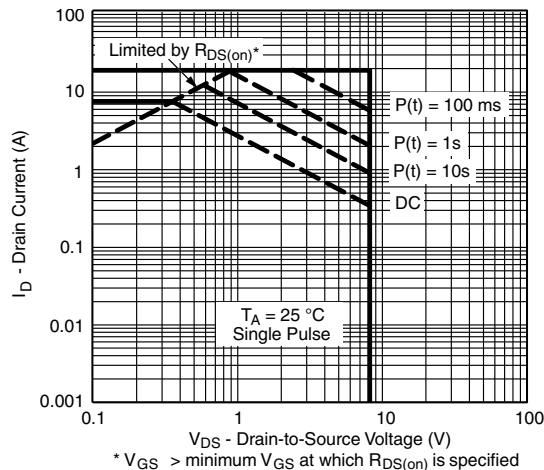
Single Pulse Power, Junction-to-Ambient



Current Derating**

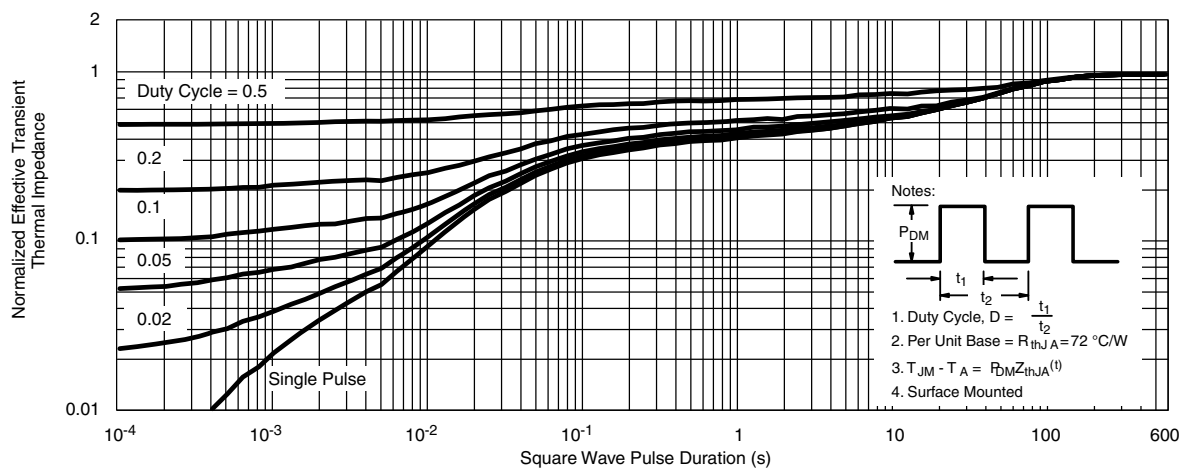
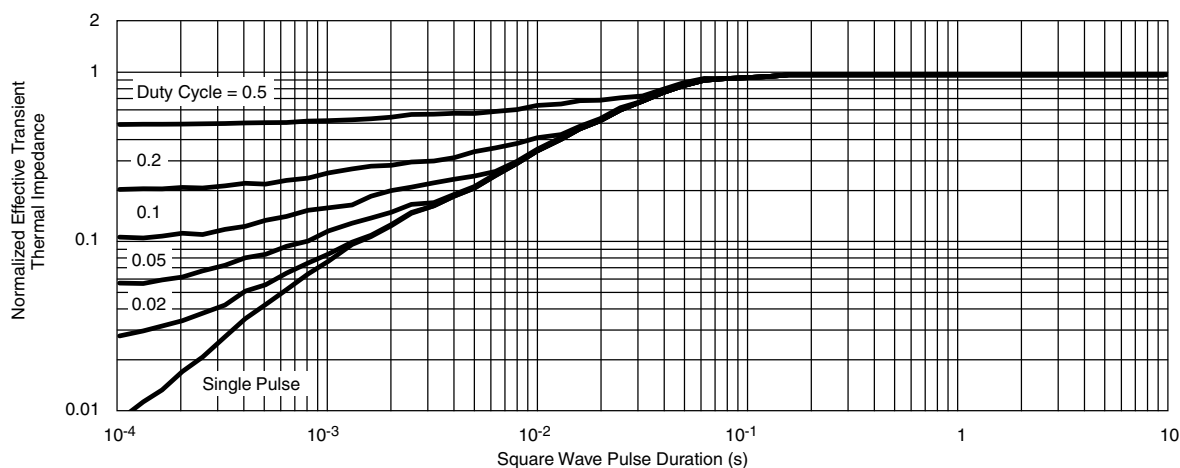


Power Derating



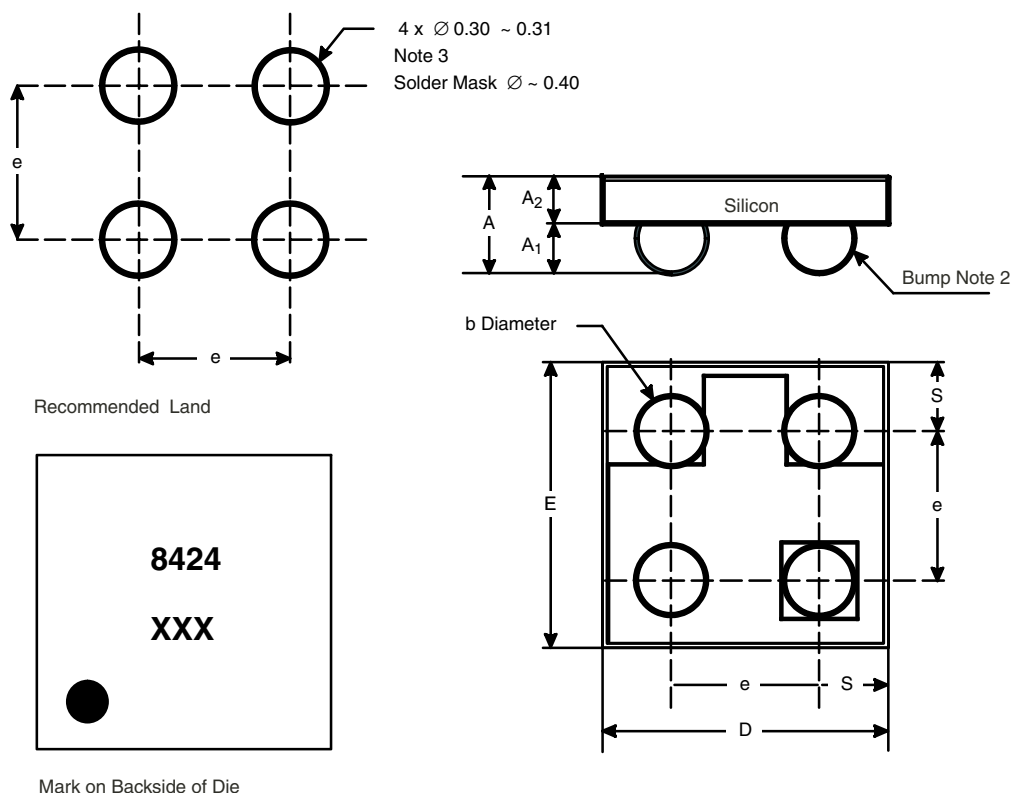
Safe Operating Area, Junction-to-Ambient

** The power dissipation P_D is based on $T_{J(max)} = 150^\circ\text{C}$, using junction-to-foot thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot

PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (0.8-mm PITCH)



Notes (unless otherwise specified):

1. Laser mark on the silicon die back, coated with a thin metal.
2. Bumps are Sn/Ag/Cu.
3. Non-solder mask defined copper landing pad.
4. The flat side of wafers is oriented at the bottom.

Dim.	Millimeters ^a		Inches	
	Min.	Max.	Min.	Max.
A	0.600	0.650	0.0236	0.0256
A ₁	0.260	0.290	0.0102	0.0114
A ₂	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	1.520	1.600	0.0598	0.0630
e	0.800		0.0315	
S	0.360	0.400	0.0142	0.0157

Note:

- a. Use millimeters as the primary measurement.

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