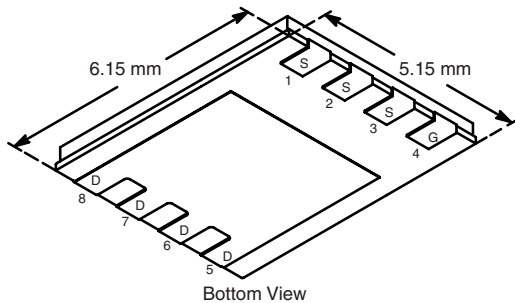


N-Channel 30-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
30	0.0087 at $V_{GS} = 10$ V	20	21
	0.010 at $V_{GS} = 4.5$ V	20	

PowerPAK SO-8



Bottom View

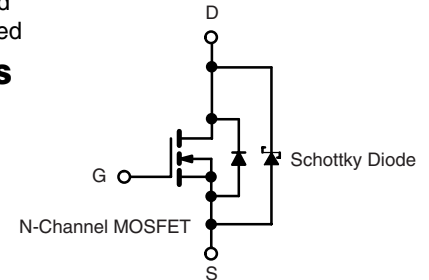
Ordering Information: Si7160DP-T1-E3 (Lead (Pb)-free)
Si7160DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- Ultra-Low On-Resistance Using High Density TrenchFET[®] Gen II Power MOSFET Technology
- Q_g Optimized
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- 100 % R_g Tested
- 100 % UIS Tested

APPLICATIONS

- Notebook
- Logic DC/DC



RoHS
COMPLIANT
HALOGEN
FREE
Available

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 16	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	20 ^a
		$T_C = 70$ °C	20 ^a
		$T_A = 25$ °C	17.8 ^{b, c}
		$T_A = 70$ °C	14.2 ^{b, c}
Pulsed Drain Current	I_{DM}	60	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	20 ^a
		$T_A = 25$ °C	4.5 ^{b, c}
Avalanche Current	I_{AS}	20	
Single Pulse Avalanche Energy	E_{AS}	20	mJ
Maximum Power Dissipation	P_D	$T_C = 25$ °C	27.7
		$T_C = 70$ °C	17.7
		$T_A = 25$ °C	5 ^{b, c}
		$T_A = 70$ °C	3.2 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	3.4	4.5	

Notes:

- Package Limited.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See Solder Profile (www.vishay.com/doc?73461). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 70 °C/W.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 16 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V		0.26	1	mA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 100 °C		12	100	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A		0.0072	0.0087	Ω
		V _{GS} = 4.5 V, I _D = 10 A		0.0083	0.010	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 15 A		60		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		2970		pF
Output Capacitance	C _{oss}			475		
Reverse Transfer Capacitance	C _{rss}			180		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A		44	66	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A		21	32	
Gate-Source Charge	Q _{gs}			6.9		
Gate-Drain Charge	Q _{gd}			5.8		
Gate Resistance	R _g	f = 1 MHz		1.0	1.5	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		29	45	ns
Rise Time	t _r			115	175	
Turn-Off Delay Time	t _{d(off)}			43	65	
Fall Time	t _f			21	35	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		15	25	
Rise Time	t _r			12	20	
Turn-Off Delay Time	t _{d(off)}			33	50	
Fall Time	t _f			8	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			20	A
Pulse Diode Forward Current ^a	I _{SM}				60	
Body Diode Voltage	V _{SD}	I _S = 2 A		0.36	0.42	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 4 A, dl/dt = 100 A/μs, T _J = 25 °C		29	45	ns
Body Diode Reverse Recovery Charge	Q _{rr}			21	35	nC
Reverse Recovery Fall Time	t _a			15		ns
Reverse Recovery Rise Time	t _b			14		

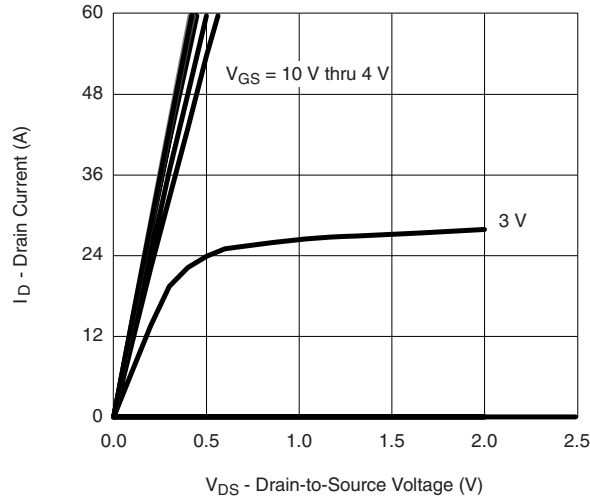
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

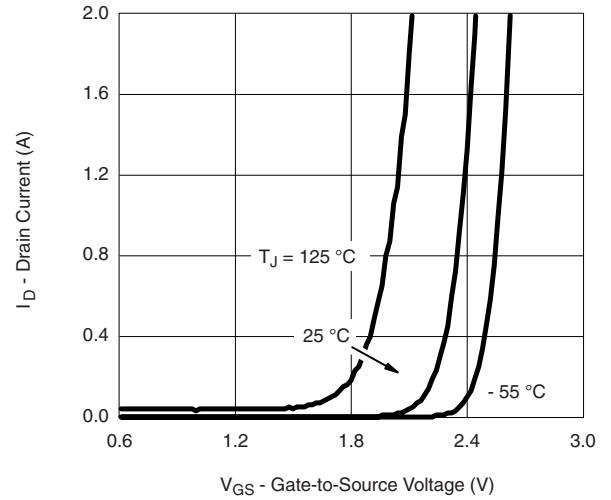
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

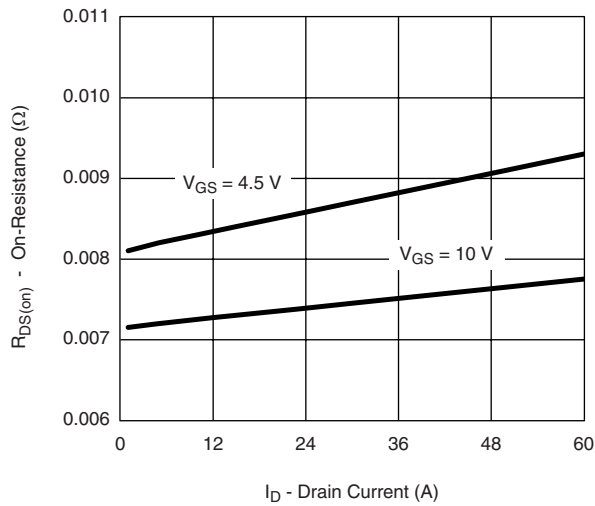
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



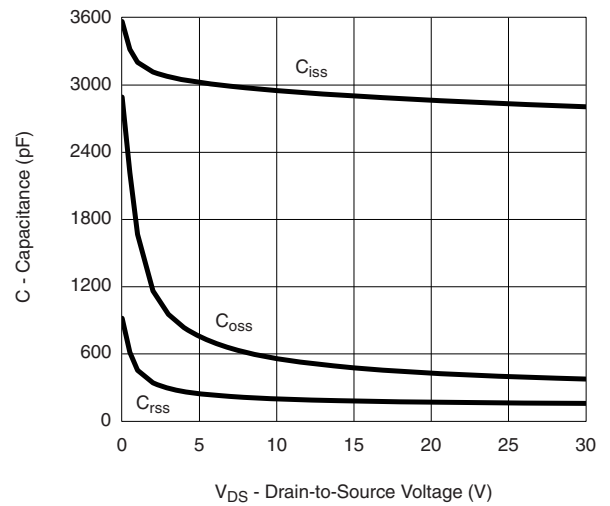
Output Characteristics



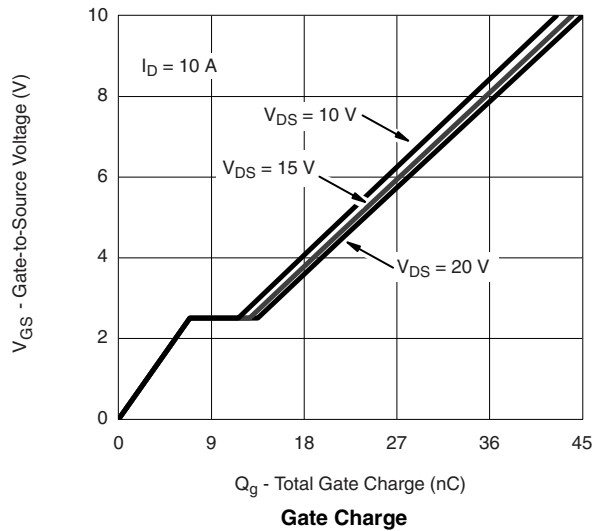
Transfer Characteristics



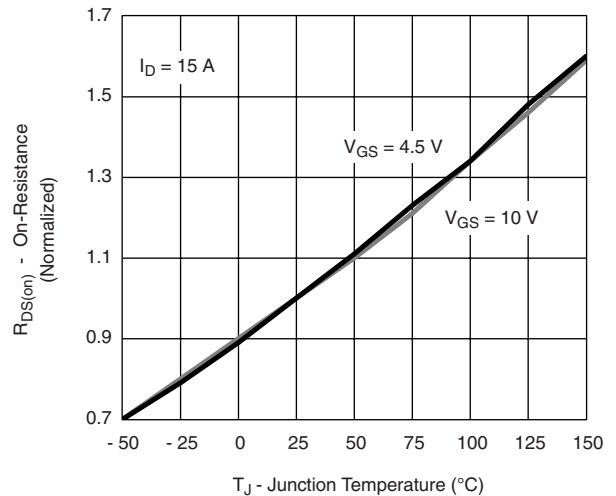
On-Resistance vs. Drain Current and Gate Voltage



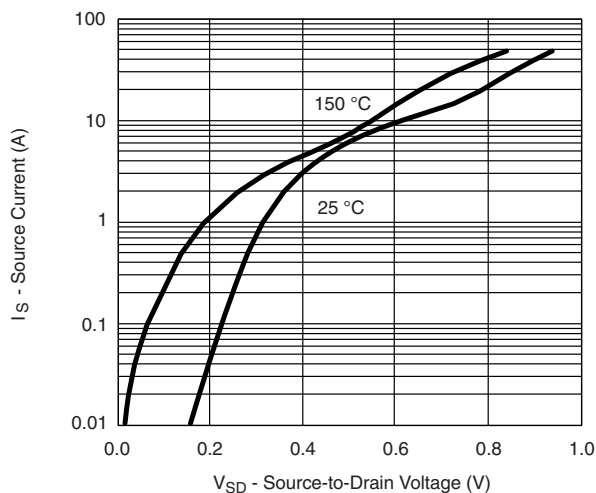
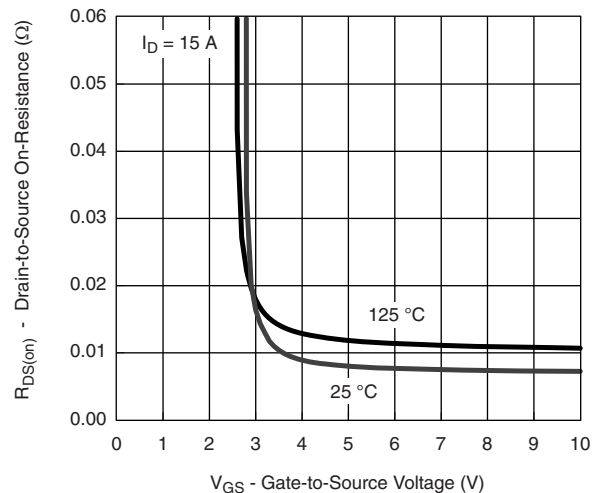
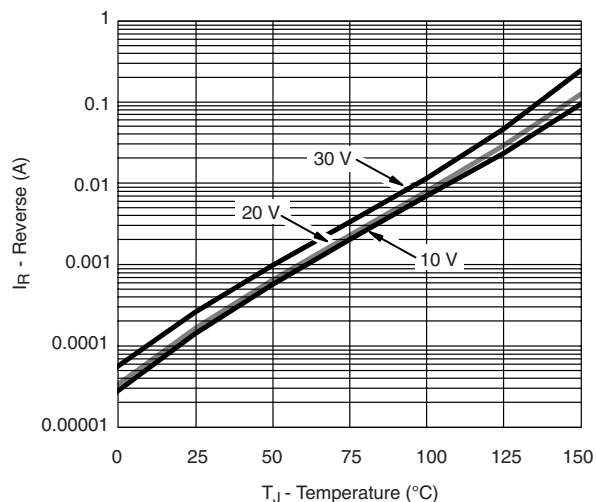
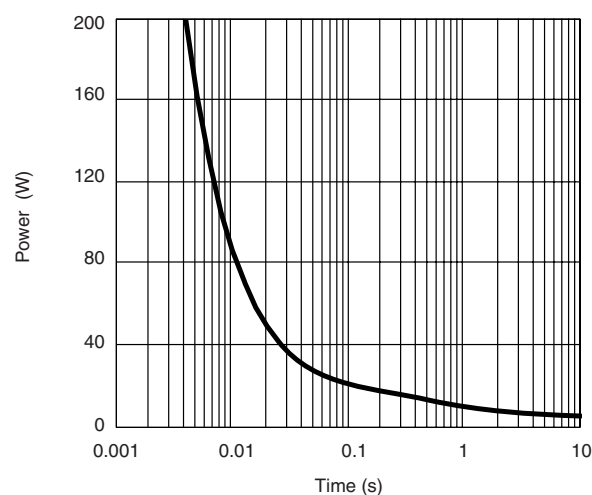
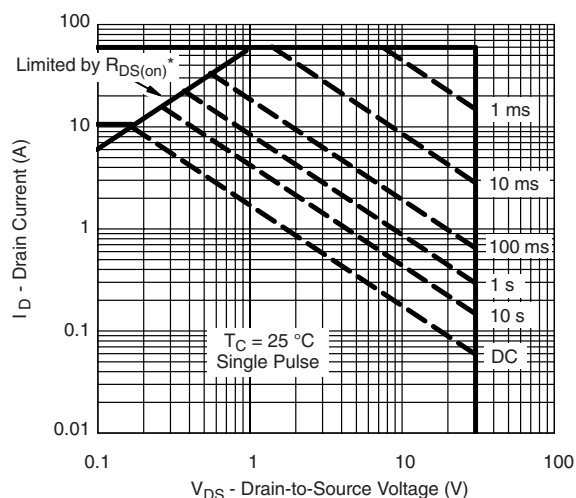
Capacitance



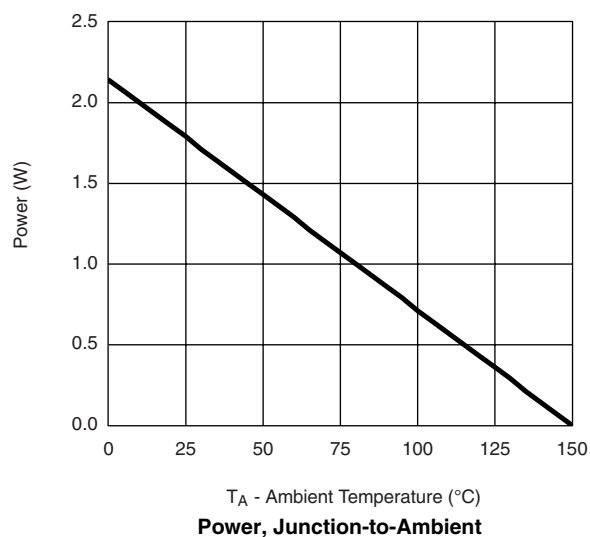
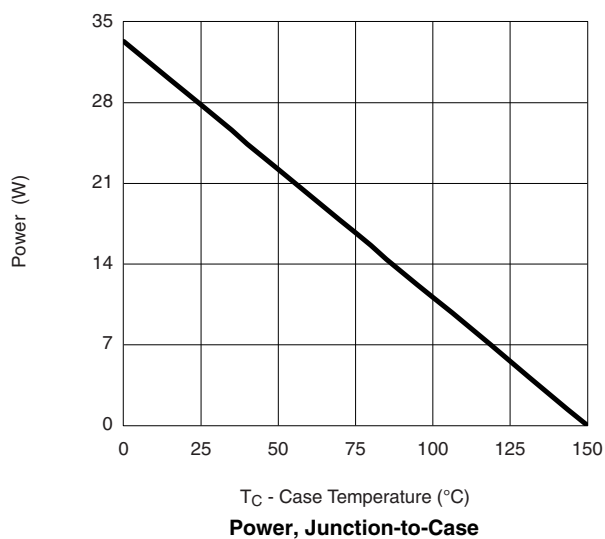
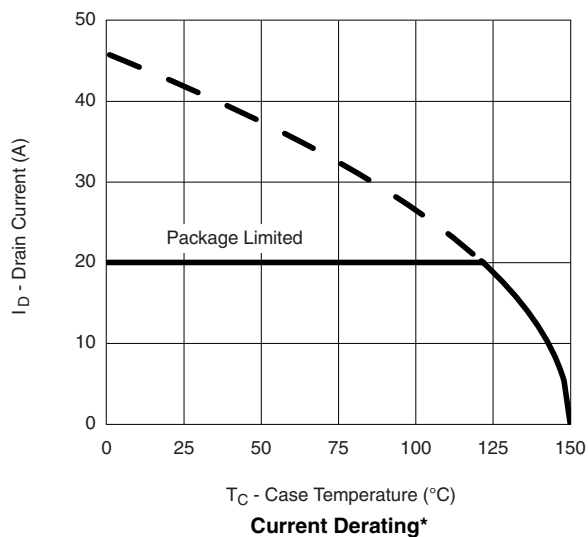
Gate Charge



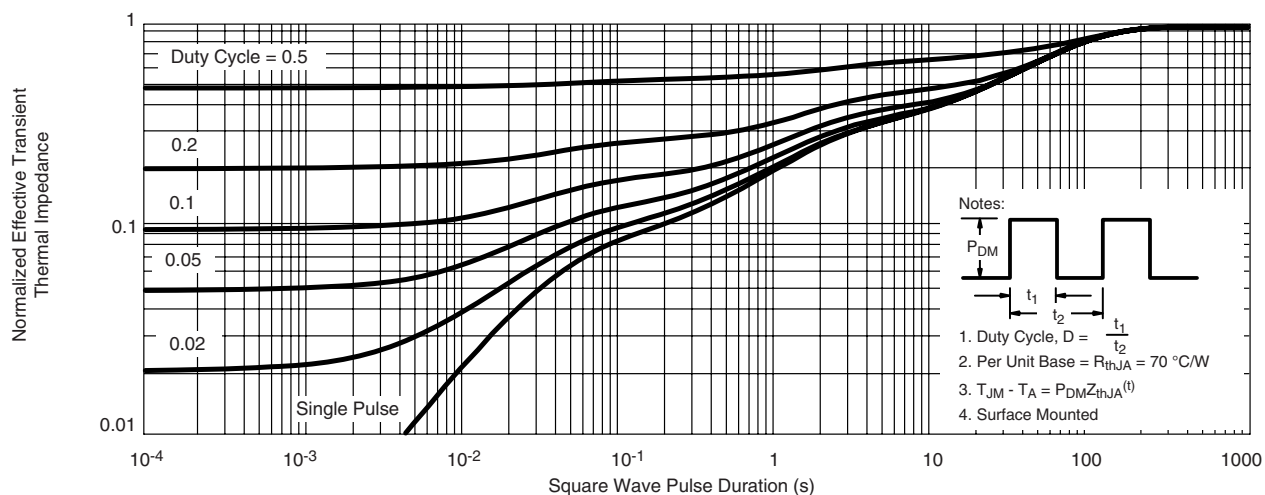
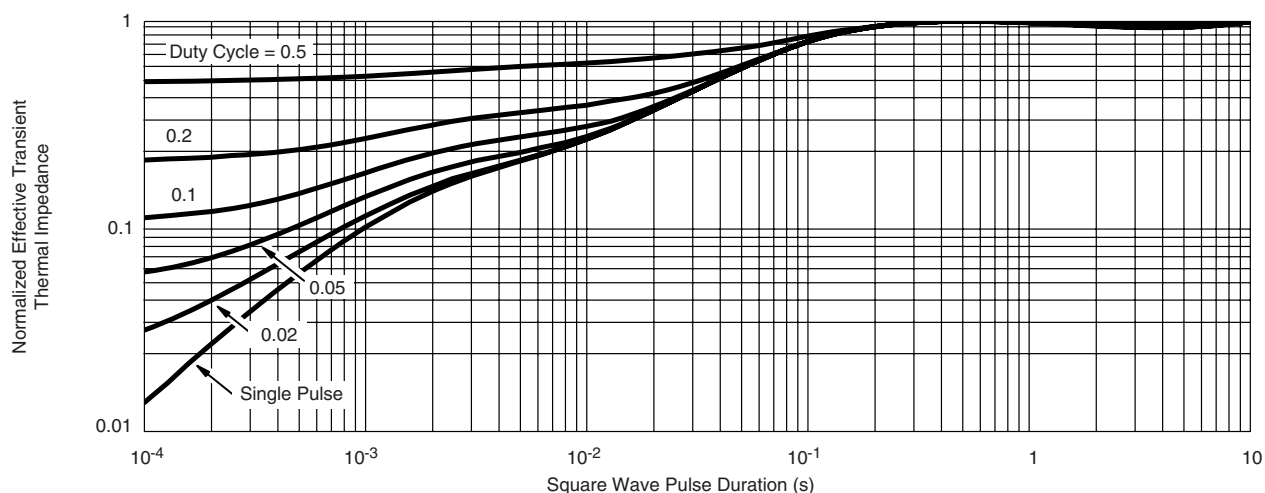
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Reverse Current (Schottky)****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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