

Dual P-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY

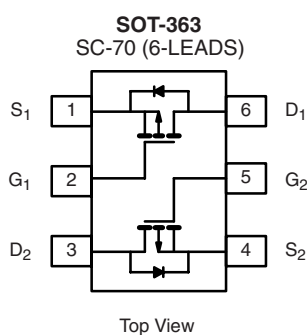
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 8	0.600 at $V_{GS} = - 4.5$ V	± 0.60
	0.850 at $V_{GS} = - 2.5$ V	± 0.50
	1.200 at $V_{GS} = - 1.8$ V	± 0.42

FEATURES

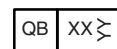
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- 1.8 V Rated
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available



Marking Code



Lot Traceability
and Date Code

Part # Code

Ordering Information: Si1905DL-T1-E3 (Lead (Pb)-free)
Si1905DL-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

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Parameter		Symbol	5 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	- 8		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	± 0.60	± 0.57	A
	T _A = 85 °C		± 0.43	± 0.41	
Pulsed Drain Current		I _{DM}	± 1.0		
Continuous Diode Current (Diode Conduction) ^a		I _S	- 0.25	- 0.23	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	0.30	0.27	W
	T _A = 85 °C		0.16	0.14	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	360	415	$^\circ\text{C/W}$
		400	460	
Maximum Junction-to-Foot (Drain)	R_{thJF}	300	350	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

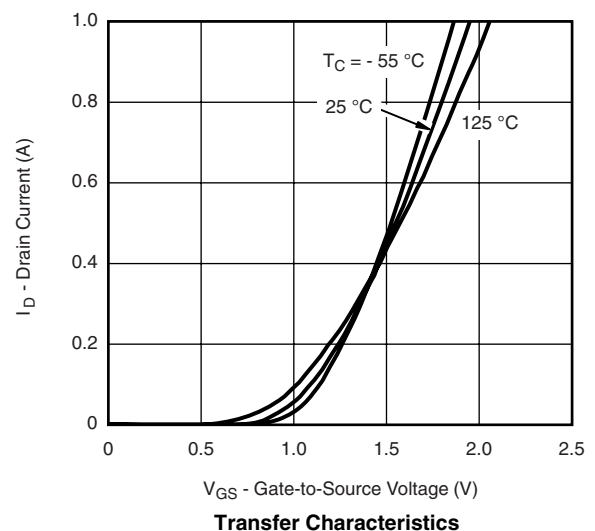
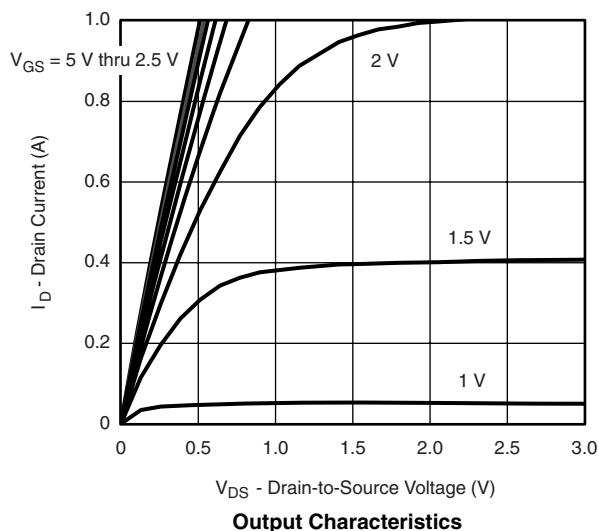
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-0.45			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -6.4\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -6.4\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 85^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}$, $V_{GS} = -4.5\ \text{V}$	-1.0			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\ \text{V}$, $I_D = -0.57\ \text{A}$		0.51	0.600	Ω
		$V_{GS} = -2.5\ \text{V}$, $I_D = -0.48\ \text{A}$		0.720	0.850	
		$V_{GS} = -1.8\ \text{V}$, $I_D = -0.20\ \text{A}$		1.0	1.200	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\ \text{V}$, $I_D = -0.57\ \text{A}$		1.2		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -0.23\ \text{A}$, $V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -4\ \text{V}$, $V_{GS} = -4.5\ \text{V}$, $I_D = -0.57\ \text{A}$		1.5	2.3	nC
Gate-Source Charge	Q_{gs}			0.17		
Gate-Drain Charge	Q_{gd}			0.16		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4\ \text{V}$, $R_L = 8\ \Omega$ $I_D \approx -0.5\ \text{A}$, $V_{GEN} = -4.5\ \text{V}$, $R_g = 6\ \Omega$		6	12	ns
Rise Time	t_r			25	50	
Turn-Off Delay Time	$t_{d(off)}$			10	20	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -0.23\ \text{A}$, $dI/dt = 100\ \text{A}/\mu\text{s}$		20	40	

Notes:

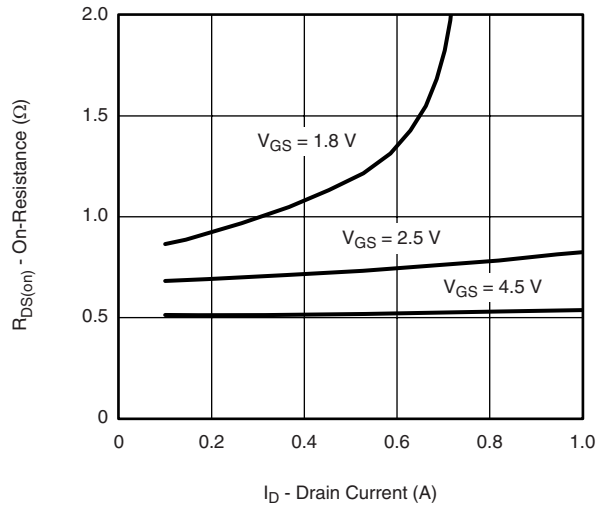
a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

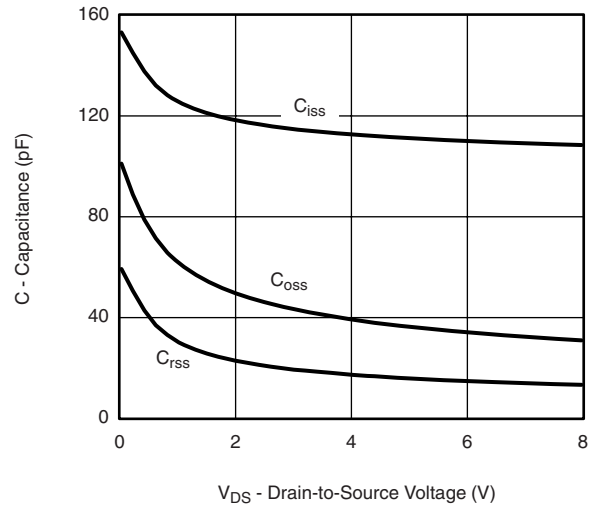
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

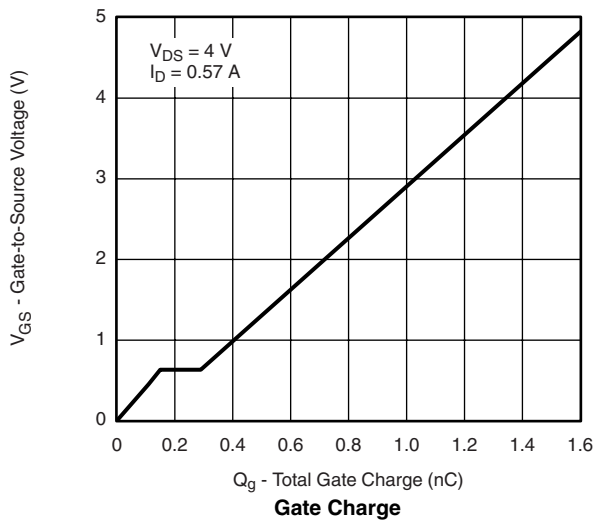
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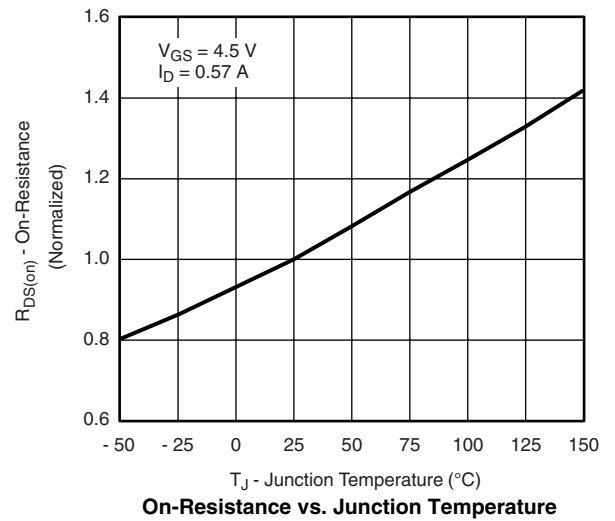
On-Resistance vs. Drain Current



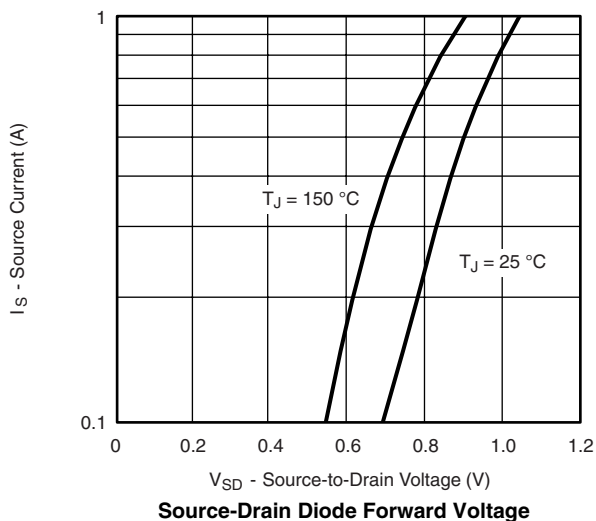
Capacitance



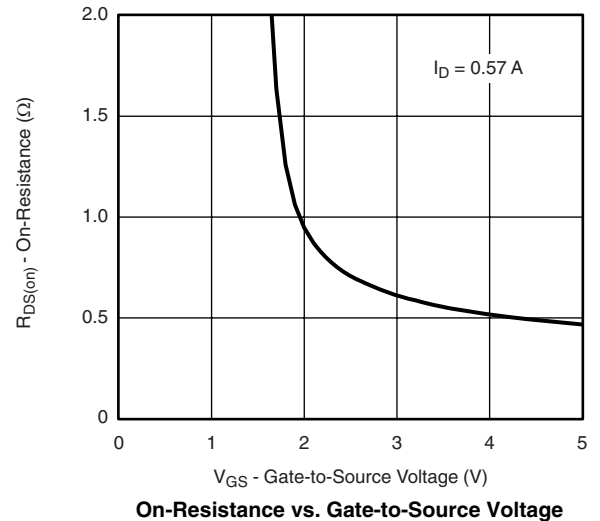
Gate Charge



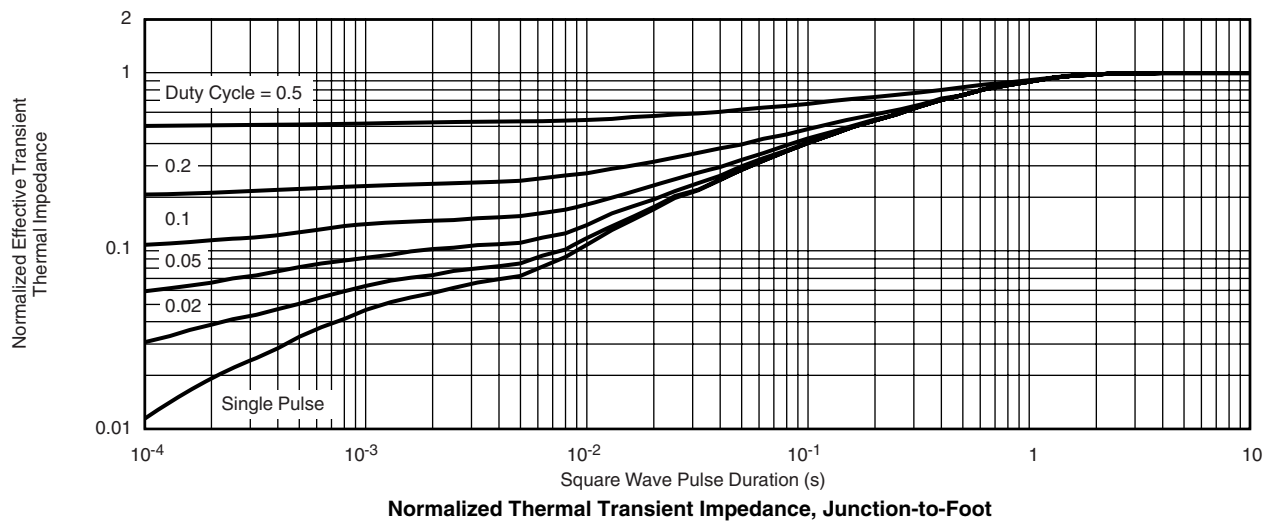
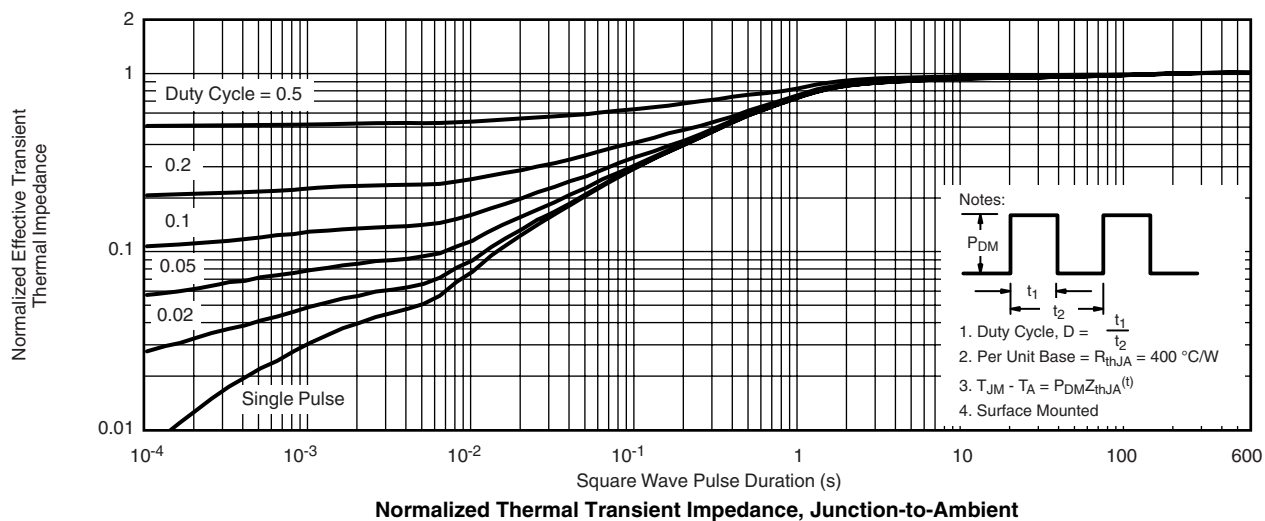
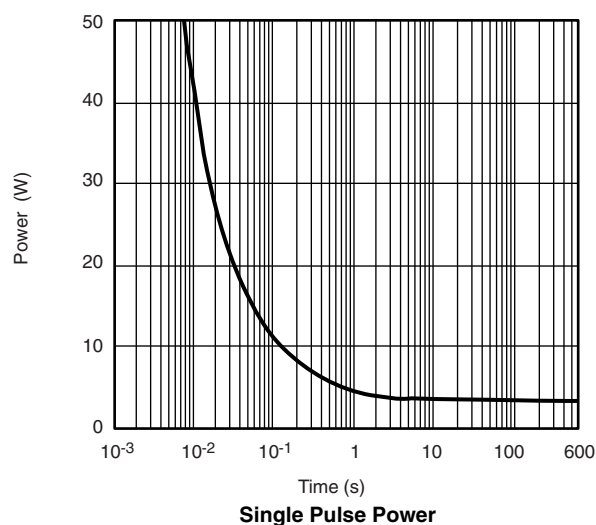
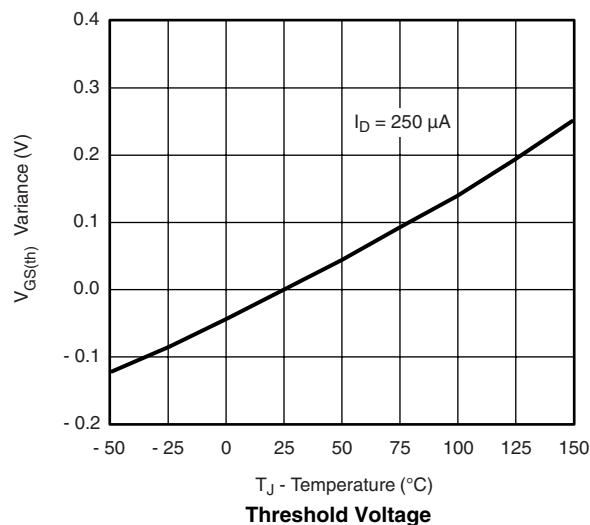
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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