

MOSFET - Symmetrical Dual N-Channel

40 V, 4.5 mΩ, 60 A

NTTFD4D0N04HL

General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q2) and synchronous (Q1) have been designed to provide optimal power efficiency.

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 4.5 mΩ at $V_{GS} = 10$ V, $I_D = 10$ A
- Max $r_{DS(on)}$ = 7 mΩ at $V_{GS} = 4.5$, $I_D = 8.0$ A

Q2: N-Channel

- Max $r_{DS(on)}$ = 4.5 mΩ at $V_{GS} = 10$ V, $I_D = 10$ A
- Max $r_{DS(on)}$ = 7 mΩ at $V_{GS} = 4.5$, $I_D = 8.0$ A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- RoHS Compliant

Typical Applications

- Computing
- Communications
- General Purpose Point of Load

PIN DESCRIPTION

Pin	Name	Description
1, 11, 12	GND (LSS)	Low Side Source
2	LSG	Low Side Gate
3, 4, 5, 6	V+ (HSD)	High Side Drain
7	HSG	High Side Gate
8, 9, 10	SW	Switching Node, Low Side Drain

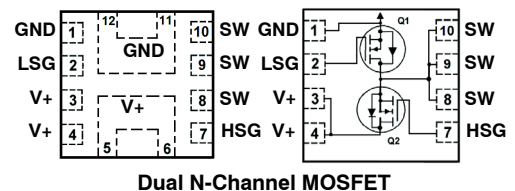


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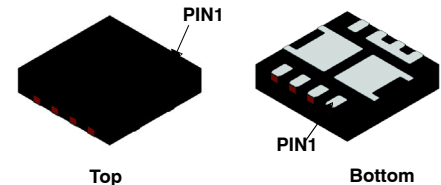
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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
40 V	4.5 mΩ @ 10 V	60 A
	7 mΩ @ 4.5 V	

ELECTRICAL CONNECTION



Dual N-Channel MOSFET



WQFN12, 3x3
CASE 510CJ

MARKING DIAGRAM



D4D0 = Specific Device Code
A = Assembly Plant Code
Y = Numeric Year Code
WW = Work Week Code
ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping†
NTTFD4D0N04HLTWG	WQFN12 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTTFD4D0N04HL

MOSFET MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter	Q1	Q2	Units
V _{DS}	Drain-to-Source Voltage	40	40	V
V _{GS}	Gate-to-Source Voltage	±20	±20	V
I _D	Drain Current –Continuous T _C = 25°C (Note 4)	60	60	A
	–Continuous T _C = 100°C (Note 4)	37	37	
	–Continuous T _A = 25°C	15 (Note 1a)	15 (Note 1b)	
	–Pulsed T _A = 25°C	349	349	
E _{AS}	Single Pulse Avalanche Energy (Note 3)	67	67	mJ
P _D	Power Dissipation for Single Operation T _C = 25°C	26	26	W
	Power Dissipation for Single Operation T _A = 25°C	1.7 (Note 1a)	1.7 (Note 1b)	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Units
R _{θJC}	Thermal Resistance, Junction-to-Case	4.8	4.8	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a), max copper	70 (Note 1a)	70 (Note 1b)	
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1c), min copper	135 (Note 1a)	135 (Note 1b)	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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OFF CHARACTERISTICS

BV _{DSS}	Drain-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	Q1	40			V
		I _D = 250 μA, V _{GS} = 0 V	Q2	40			
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	Q1		16.63		mV/°C
		I _D = 250 μA, referenced to 25°C	Q2		16.63		
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 40 V, V _{GS} = 0 V	Q1			10	μA
		V _{DS} = 40 V, V _{GS} = 0 V	Q2			10	
I _{GSS}	Gate-to-Source Leakage Current, Forward	V _{GS} = +20/-16 V, V _{DS} = 0 V	Q1			±100	nA
		V _{GS} = +20/-16 V, V _{DS} = 0 V	Q2			±100	

ON CHARACTERISTICS

V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 50 μA	Q1	1.2	1.5	2.0	V
		V _{GS} = V _{DS} , I _D = 50 μA	Q2	1.2	1.5	2.0	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate-to-Source Threshold Voltage Temperature Coefficient	I _D = 50 μA, referenced to 25°C	Q1		–5.75		mV/°C
		I _D = 50 μA, referenced to 25°C	Q2		–5.75		
r _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 10 A	Q1		3.7	4.5	mΩ
		V _{GS} = 4.5 V, I _D = 8 A			5.8	7	
		V _{GS} = 10 V, I _D = 10 A, T _J = 125°C			6.4		
r _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 10 A	Q2		3.7	4.5	mΩ
		V _{GS} = 4.5 V, I _D = 8 A			5.8	7	
		V _{GS} = 10 V, I _D = 10 A, T _J = 125°C			6.4		
g _{FS}	Forward Transconductance	V _{DS} = 15 V, I _D = 10 A	Q1		61		S
		V _{DS} = 15 V, I _D = 10 A	Q2		61		

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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DYNAMIC CHARACTERISTICS

C_{ISS}	Input Capacitance	Q1: $V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	Q1		1100		pF
			Q2		1100		
C_{OSS}	Output Capacitance	Q2: $V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	Q1		271		pF
			Q2		271		
C_{RSS}	Reverse Transfer Capacitance		Q1		22		pF
			Q2		22		
R_G	Gate Resistance	$T_A = 25^\circ\text{C}$	Q1		2.0		Ω
			Q2		2.0		

SWITCHING CHARACTERISTICS

td(ON)	Turn-On Delay Time	Q1: VDD = 32 V, ID = 30.5 A, VGS = 4.5 V, RGEN = 2.5 Ω Q2: VDD = 32 V, ID = 30.5 A, VGS = 4.5 V, RGEN = 2.5 Ω	Q1		9.5		ns	
			Q2		9.5			
tr	Rise Time		Q1		5.6		ns	
			Q2		5.6			
tD(OFF)	Turn-Off Delay Time		Q1		1.7		ns	
			Q2		1.7			
tf	Fall Time		Q1		5.8		ns	
			Q2		5.8			
Qg	Total Gate Charge		VGS = 0 V to 10 V Q1: VDD = 32 V, ID = 30.5 A Q2: VDD = 32 V, ID = 30.5 A	Q1		18		nC
				Q2		18		
Qg	Total Gate Charge	Q1			8.6		nC	
		Q2			8.6			
Qgs	Gate-to-Source Gate Charge	Q1			3.1		nC	
		Q2			3.1			
Qgd	Gate-to-Drain "Miller" Charge	Q1			3.2		nC	
		Q2			3.2			

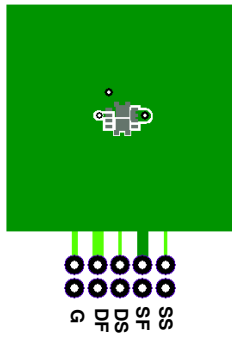
DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 10 A (Note 2)	Q1		0.78	1.2	V
		V _{GS} = 0 V, I _S = 10 A (Note 2)	Q2		0.78	1.2	
t _{rr}	Reverse Recovery Time	Q1: I _F = 30.5 A, di/dt = 100 A/μs Q2: I _F = 30.5 A, di/dt = 100 A/μs	Q1		26		ns
			Q2		26		
Q _{rr}	Reverse Recovery Charge		Q1		9		nC
			Q2		9		

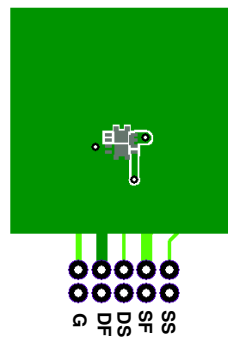
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.

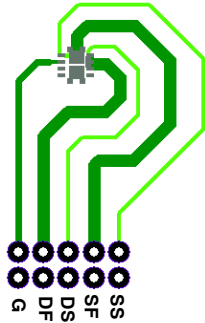
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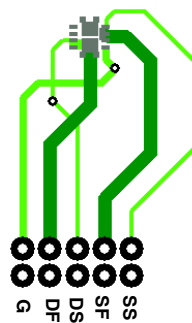
a) 70°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 70°C/W when mounted on a 1 in² pad of 2 oz copper.



c) 135°C/W when mounted on a minimum pad of 2 oz copper.



d) 135°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
3. Q1: E_{AS} of 67 mJ is based on starting T_J = 25°C; N-ch: L = 1 mH, I_{AS} = 11.6 A, V_{DD} = 40 V, V_{GS} = 10 V. 100% test at L = 1 mH, I_{AS} = 11.6 A.
Q2: E_{AS} of 67 mJ is based on starting T_J = 25°C; N-ch: L = 1 mH, I_{AS} = 11.6 A, V_{DD} = 40 V, V_{GS} = 10 V. 100% test at L = 1 mH, I_{AS} = 11.6 A.
4. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

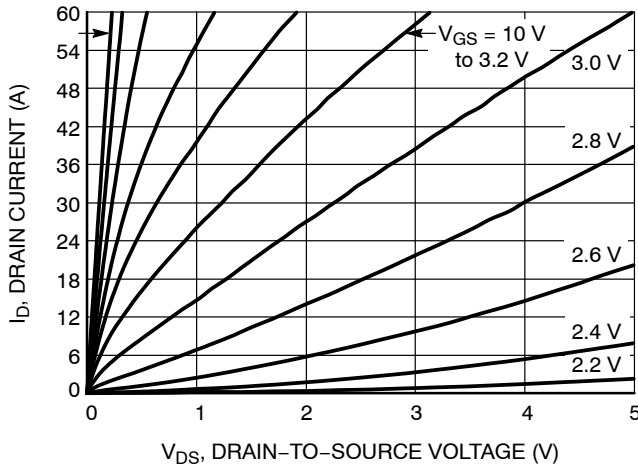


Figure 1. On-Region Characteristics

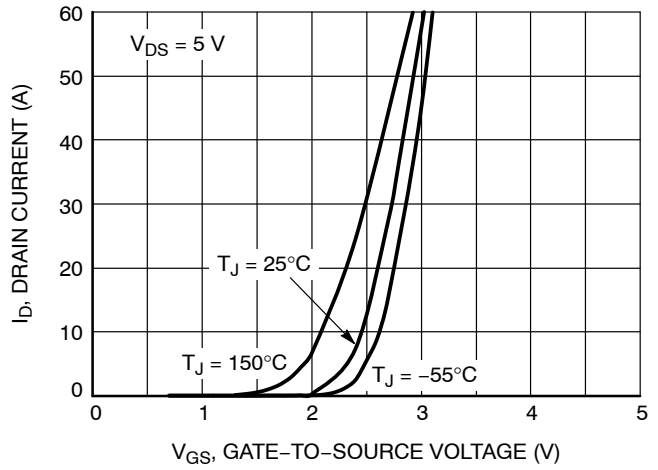


Figure 2. Transfer Characteristics

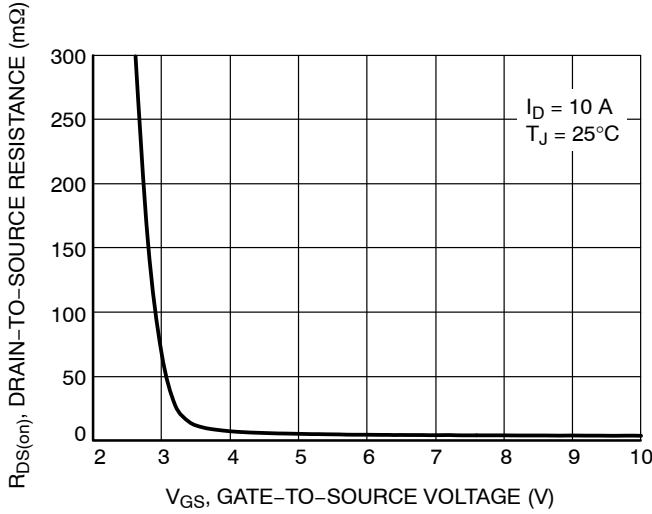


Figure 3. On-Resistance vs. Gate-to-Source Voltage

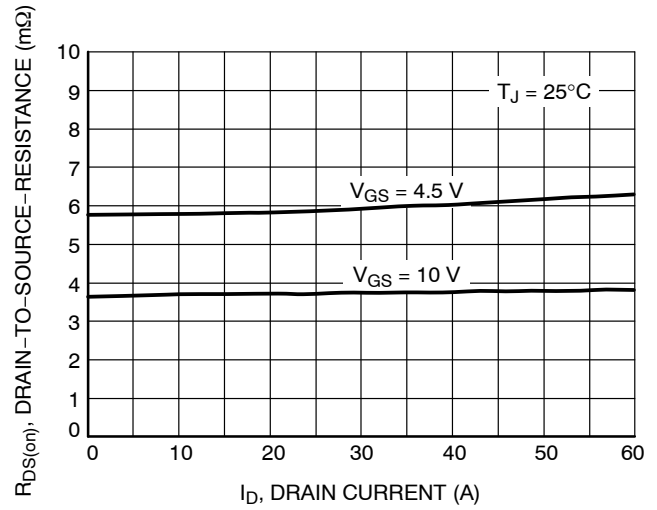


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

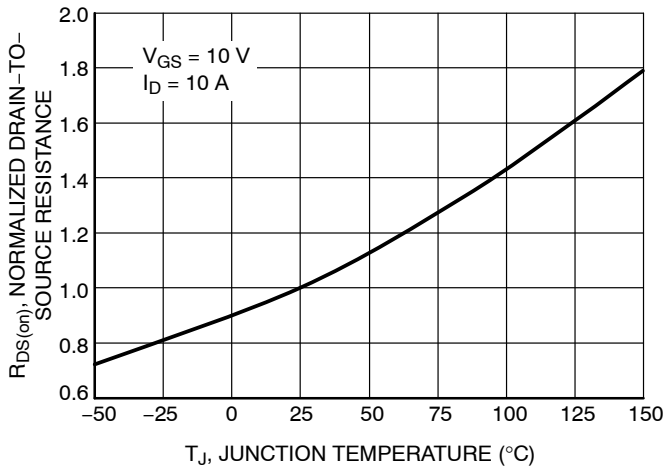


Figure 5. On-Resistance Variation with Temperature

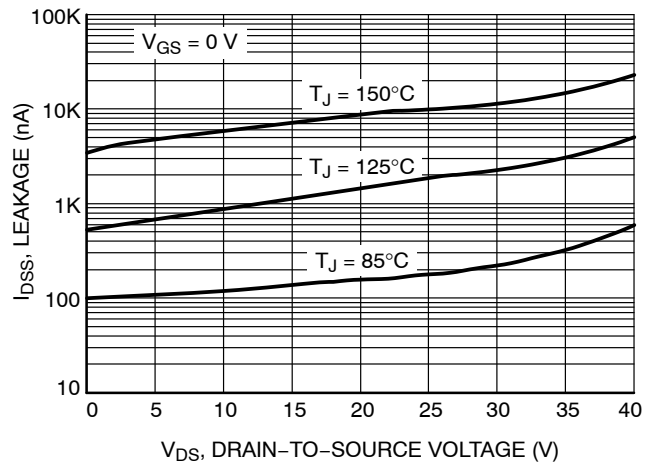


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

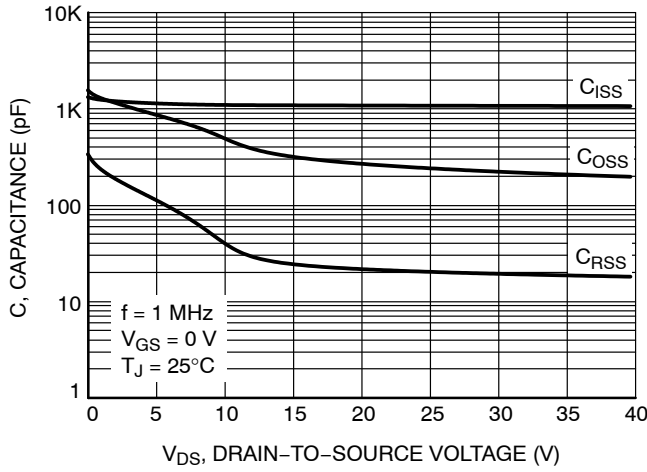


Figure 7. Capacitance Variation

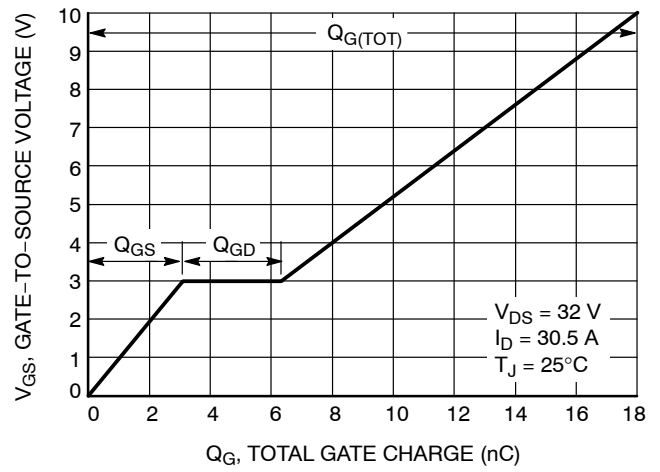


Figure 8. Gate-to-Source vs. Total Charge

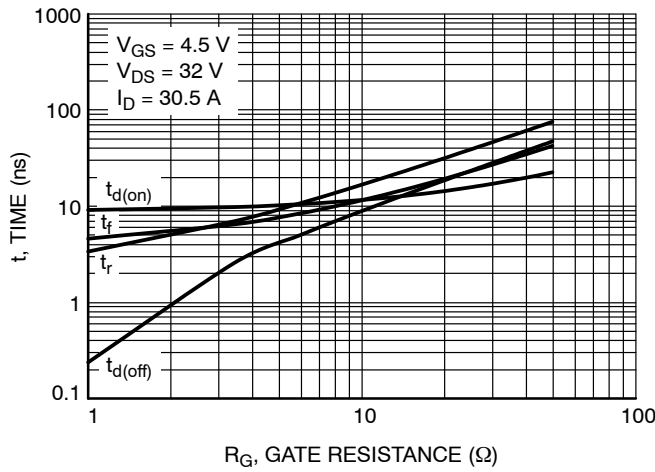


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

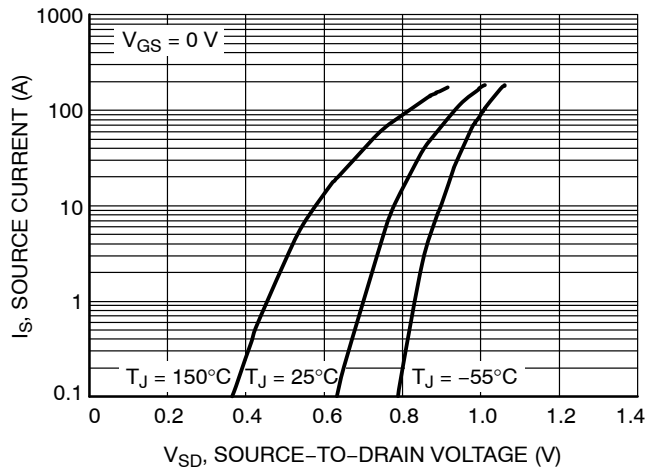


Figure 10. Diode Forward Voltage vs. Current

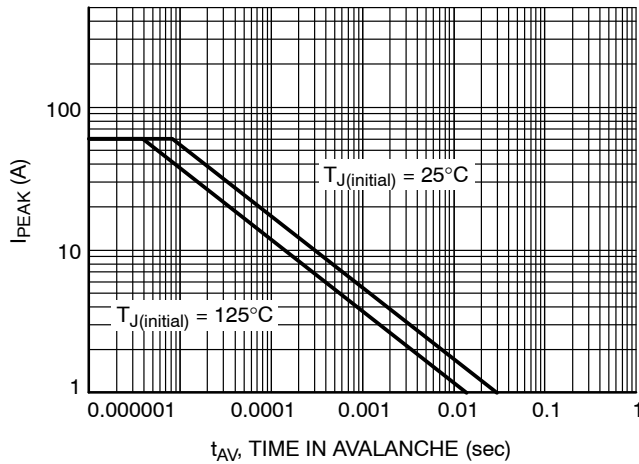


Figure 11. Unclamped Inductive Switching Capability

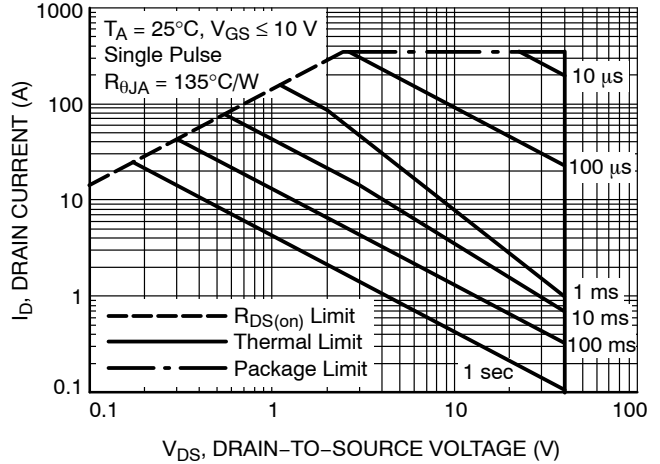


Figure 12. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS

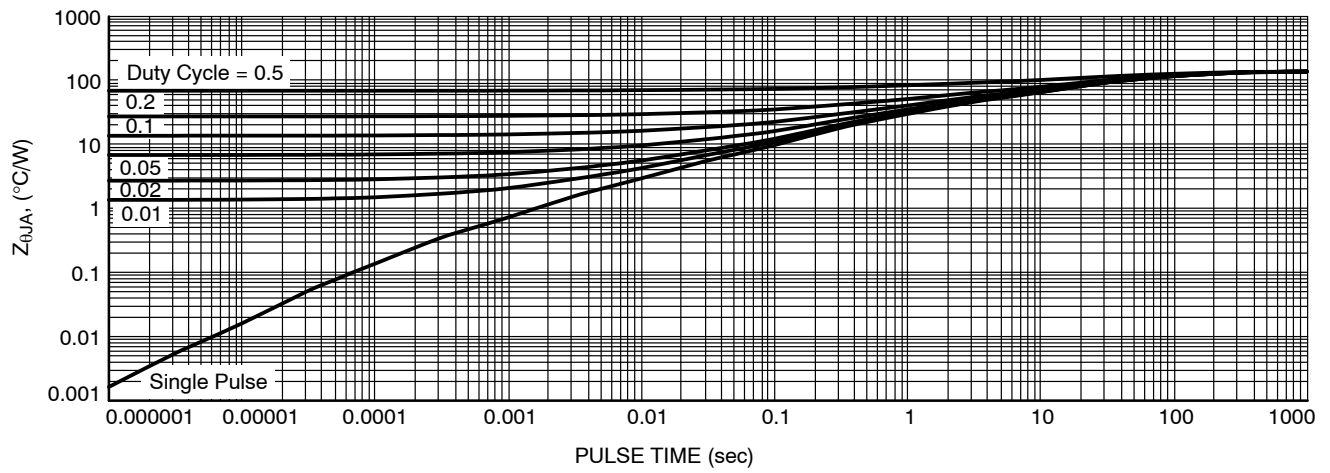
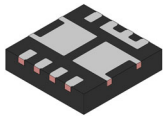


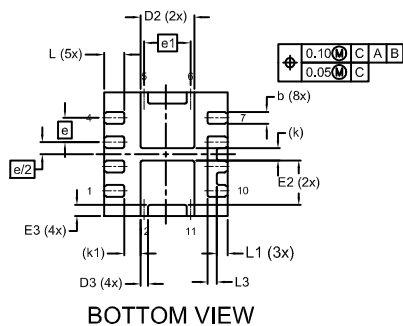
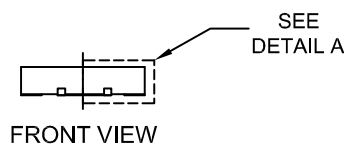
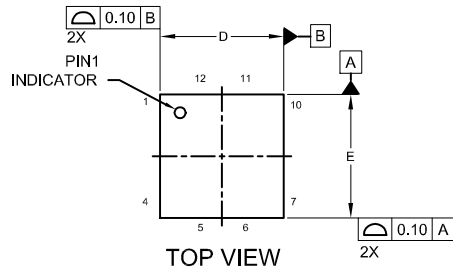
Figure 13. Transient Thermal Impedance

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

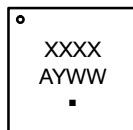


WQFN12 3.3X3.3, 0.65P CASE 510CJ ISSUE A

DATE 08 AUG 2022



GENERIC MARKING DIAGRAM*

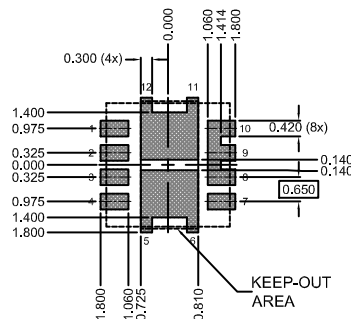
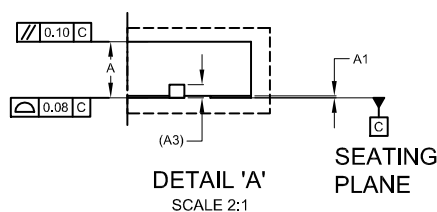


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
5. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	1.34	1.44	1.54
D3	0.10	0.20	0.30
E	3.20	3.30	3.40
E2	1.09	1.19	1.29
E3	0.20	0.30	0.40
e	0.65 BSC		
e/2	0.325 BSC		
e1	1.24 BSC		
k	0.33 REF		
k1	0.43 REF		
L	0.44	0.54	0.64
L1	0.19	0.29	0.39
L3	0.15	0.25	0.35

DOCUMENT NUMBER: 98AON13806G

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DESCRIPTION: WQFN12 3.3X3.3, 0.65P

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