

NTHC5513

MOSFET – Power, Complementary ChipFET 20 V, +3.9 A / -3.0 A

Features

- Complementary N-Channel and P-Channel MOSFET
- Small Size, 40% Smaller than TSOP-6 Package
- Leadless SMD Package Featuring Complementary Pair
- ChipFET Package Provides Great Thermal Characteristics Similar to Larger Packages
- Low $R_{DS(on)}$ in a ChipFET Package for High Efficiency Performance
- Low Profile (< 1.10 mm) Allows Placement in Extremely Thin Environments Such as Portable Electronics
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Load Switch Applications Requiring Level Shift
- DC-DC Conversion Circuits
- Drive Small Brushless DC Motors
- Designed for Power Management Applications in Portable, Battery Powered Products

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	20	V
Gate-to-Source Voltage			V _{GS}	±12	V
Continuous Drain Current (Note 1)	N-Ch Steady State	T _A = 25°C	I _D	2.9	A
		T _A = 85°C		2.1	
		t ≤ 5		3.9	
	P-Ch Steady State	T _A = 25°C	I _D	-2.2	A
		T _A = 85°C		-1.6	
		t ≤ 5		-3.0	
Pulsed Drain Current (Note 1)	N-Ch	t = 10 μs	I _{DM}	12	A
	P-Ch	t = 10 μs		-9.0	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.1	W
		t ≤ 5		2.1	
Operating Junction and Storage Temperature			T _J , T _{STG}	-55 to 150	°C
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

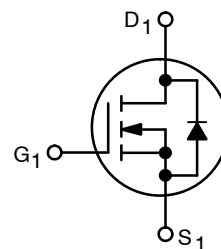
1. Surface Mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



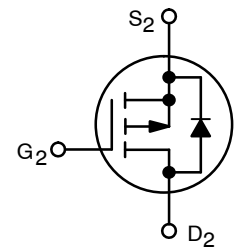
ON Semiconductor®

www.onsemi.com

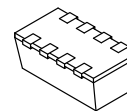
$V_{(BR)DS}$	$R_{DS(on)}$ TYP	I_D MAX
N-Channel 20 V	60 m Ω @ 4.5 V	3.9 A
	80 m Ω @ 2.5 V	
P-Channel -20 V	130 m Ω @ -4.5 V	-3.0 A
	200 m Ω @ -2.5 V	



N-Channel MOSFET

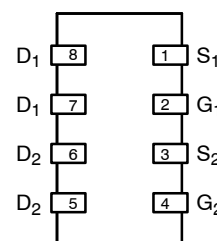


P-Channel MOSFET

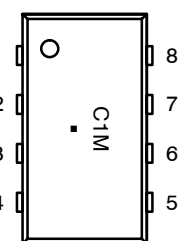


ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



MARKING DIAGRAM



C1 = Specific Device Code
M = Month Code
■ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHC5513T1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter			Symbol	Max	Unit
Junction-to-Ambient (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	$R_{\theta JA}$	110	$^{\circ}\text{C/W}$
	$t \leq 5$			60	

2. Surface Mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS (Note 3)

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	N	$V_{GS} = 0\text{ V}$	$I_D = 250\text{ }\mu\text{A}$	20		V
		P		$I_D = -250\text{ }\mu\text{A}$	-20		
Zero Gate Voltage Drain Current	I_{DSS}	N	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}$			1.0	μA
		P	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$			-1.0	
		N	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}, T_J = 85^{\circ}\text{C}$			5	
		P	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}, T_J = 85^{\circ}\text{C}$			-5	
Gate-to-Source Leakage Current	I_{GSS}		$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	N	$V_{GS} = V_{DS}$	$I_D = 250\text{ }\mu\text{A}$	0.6		1.2	V
		P		$I_D = -250\text{ }\mu\text{A}$	-0.6		-1.2	
Drain-to-Source On Resistance	$R_{DS(on)}$	N	$V_{GS} = 4.5\text{ V}, I_D = 2.9\text{ A}$			0.058	0.080	Ω
		P	$V_{GS} = -4.5\text{ V}, I_D = -2.2\text{ A}$			0.130	0.155	
		N	$V_{GS} = 2.5\text{ V}, I_D = 2.3\text{ A}$			0.077	0.115	
		P	$V_{GS} = -2.5\text{ V}, I_D = -1.7\text{ A}$			0.200	0.240	
Forward Transconductance	g_{FS}	N	$V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$			6.0		S
		P	$V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$			6.0		

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	N	$f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}$		180		pF
		P		$V_{DS} = -10\text{ V}$		185		
Output Capacitance	C_{OSS}	N		$V_{DS} = 10\text{ V}$		80		
		P		$V_{DS} = -10\text{ V}$		95		
Reverse Transfer Capacitance	C_{RSS}	N		$V_{DS} = 10\text{ V}$		25		
		P		$V_{DS} = -10\text{ V}$		30		
Total Gate Charge	$Q_{G(TOT)}$	N		$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		2.6	4.0	nC
		P		$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$		3.0	6.0	
Gate-to-Source Gate Charge	Q_{GS}	N		$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		0.6		
		P		$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$		0.5		
Gate-to-Drain "Miller" Charge	Q_{GD}	N		$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		0.7		
		P		$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$		0.9		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width $\leq 250\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

NTHC5513

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 4)							
Turn-On Delay Time	t _{d(ON)}	N	V _{DD} = 16 V, V _{GS} = 4.5 V, I _D = 2.9 A, R _G = 2.5 Ω		5.0	10	ns
Rise Time	t _r				9.0	18	
Turn-Off Delay Time	t _{d(OFF)}				10	20	
Fall Time	t _f				3.0	6.0	
Turn-On Delay Time	t _{d(ON)}	P	V _{DD} = -16 V, V _{GS} = -4.5 V, I _D = -2.2 A, R _G = 2.5 Ω		7.0	12	
Rise Time	t _r				13	25	
Turn-Off Delay Time	t _{d(OFF)}				33	50	
Fall Time	t _f				27	40	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage (Note 5)	V _{SD}	N	V _{GS} = 0 V	I _S = 2.6 A		0.8	1.15	V
		P		I _S = -2.1 A		-0.8	-1.15	
Reverse Recovery Time (Note 4)	t _{RR}	N	V _{GS} = 0 V, dI _S / dt = 100 A/μs	I _S = 1.5 A		12.5		ns
		P		I _S = -1.5 A		32		
Charge Time	t _a	N		I _S = 1.5 A		9.0		
		P		I _S = -1.5 A		10		
Discharge Time	t _b	N		I _S = 1.5 A		3.5		
		P		I _S = -1.5 A		22		
Reverse Recovery Charge	Q _{RR}	N		I _S = 1.5 A		6.0		nC
		P		I _S = -1.5 A		15		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures.

5. Pulse Test: Pulse Width ≤ 250 μs, Duty Cycle ≤ 2%.

TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

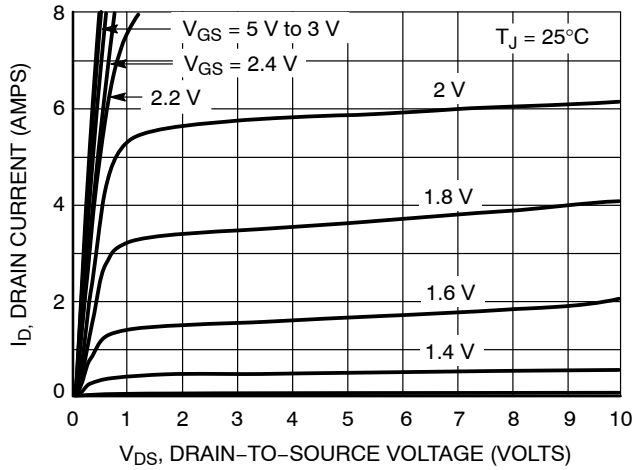


Figure 1. On-Region Characteristics

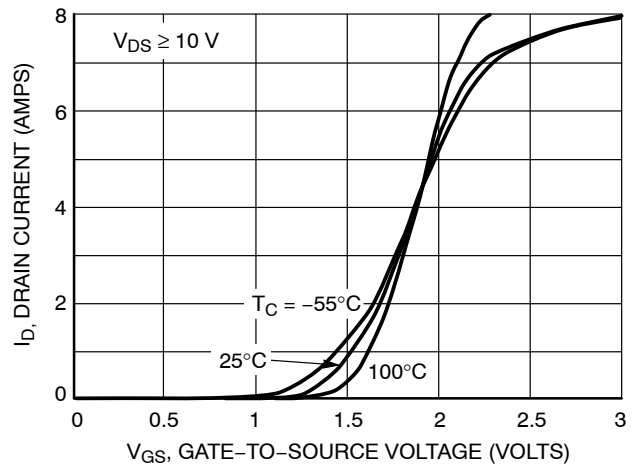


Figure 2. Transfer Characteristics

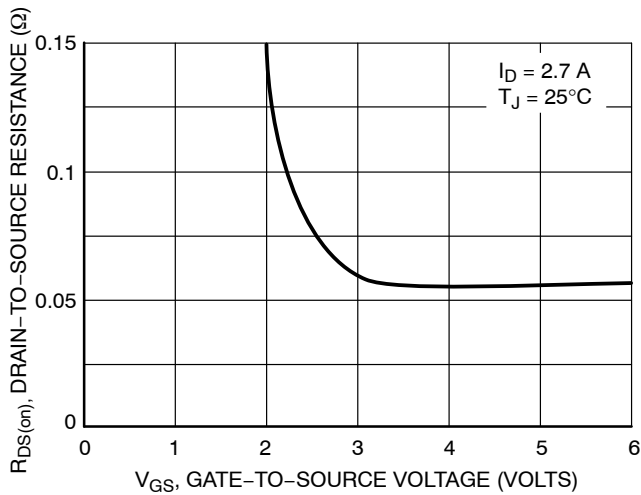


Figure 3. On-Resistance vs. Gate-to-Source Voltage

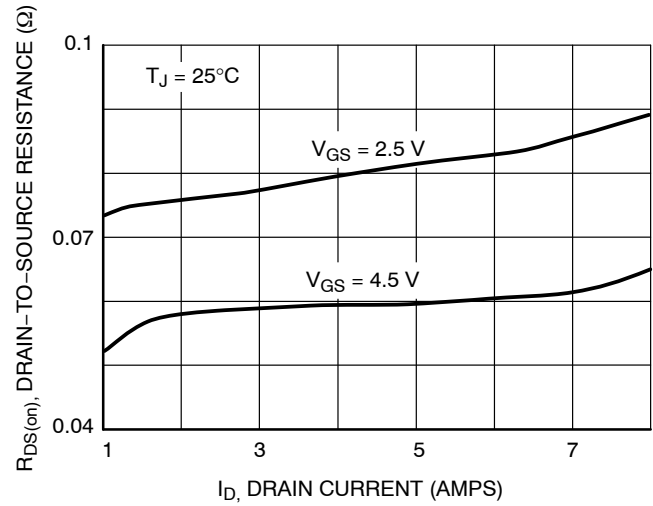


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

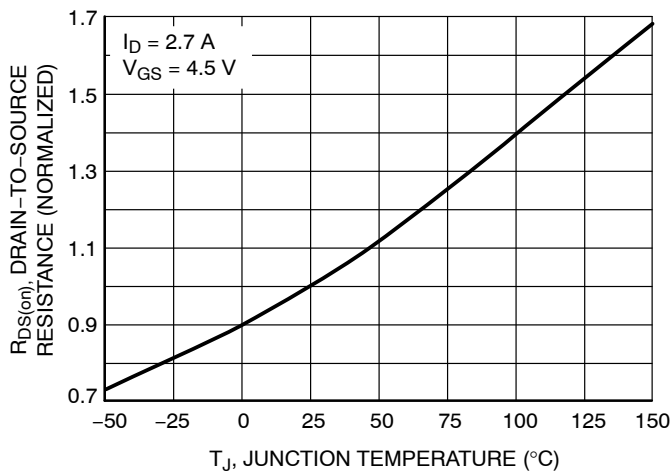


Figure 5. On-Resistance Variation with Temperature

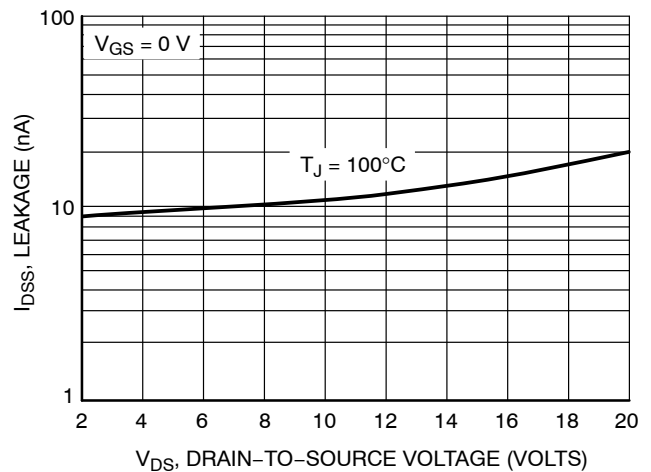
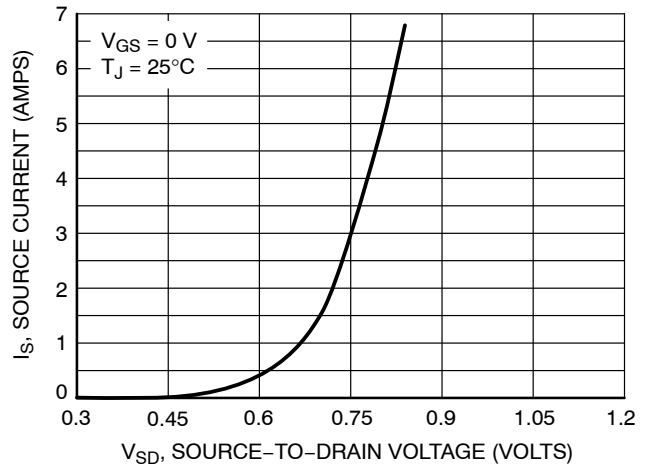
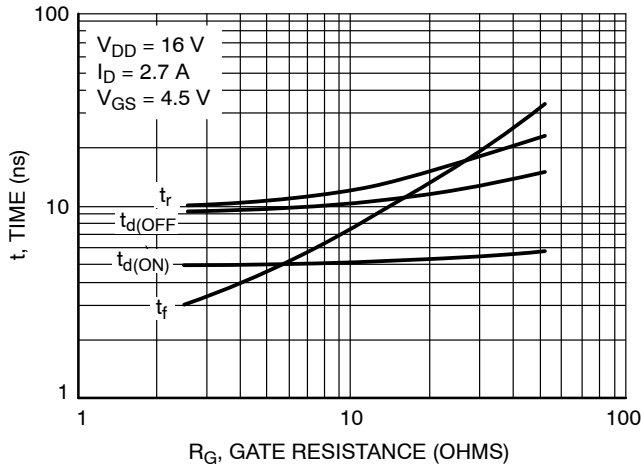
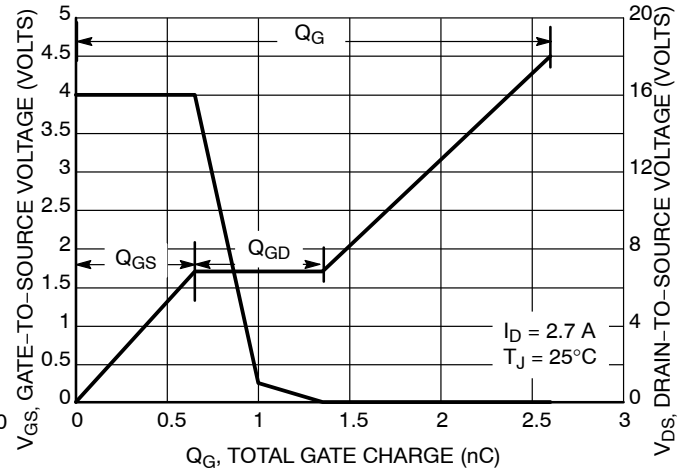
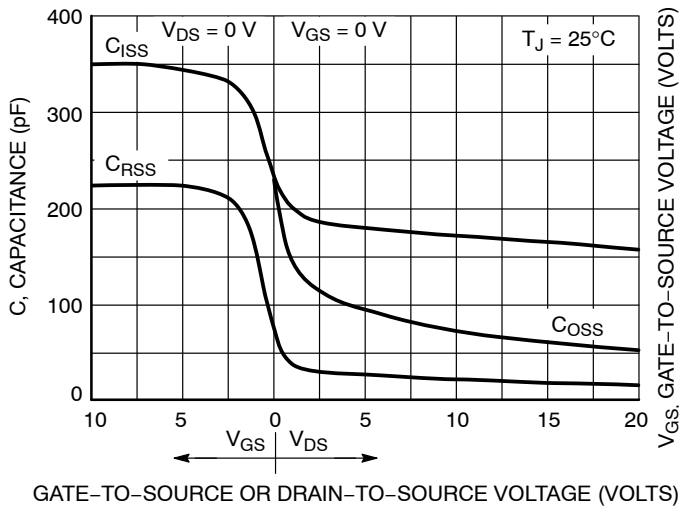


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)



TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

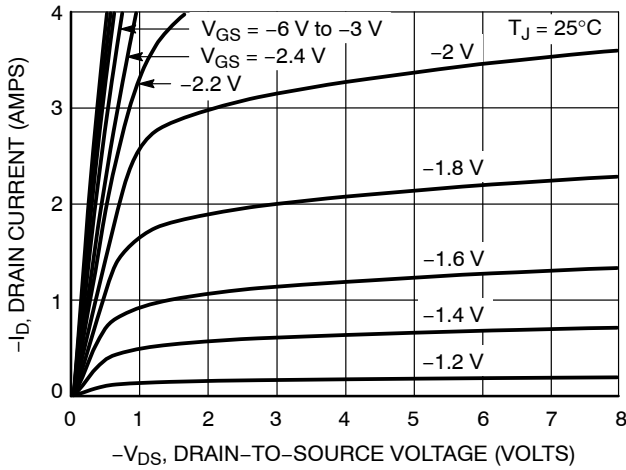


Figure 11. On-Region Characteristics

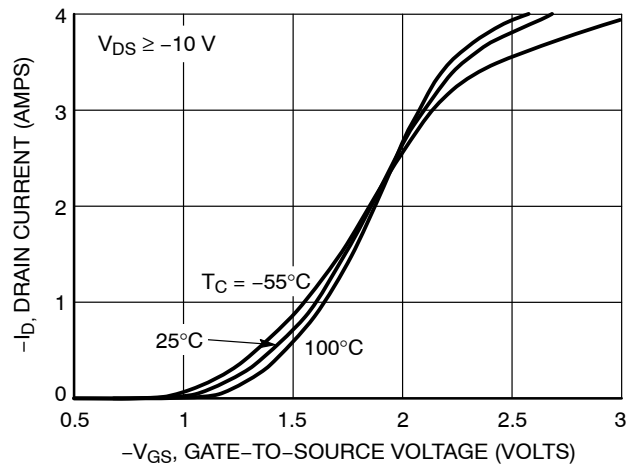


Figure 12. Transfer Characteristics

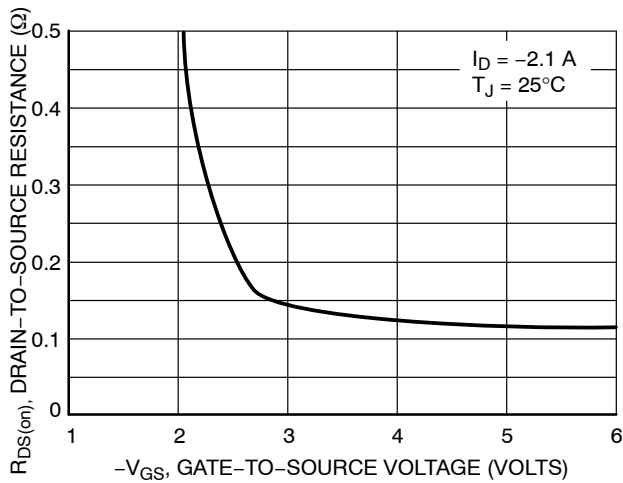


Figure 13. On-Resistance vs. Gate-to-Source Voltage

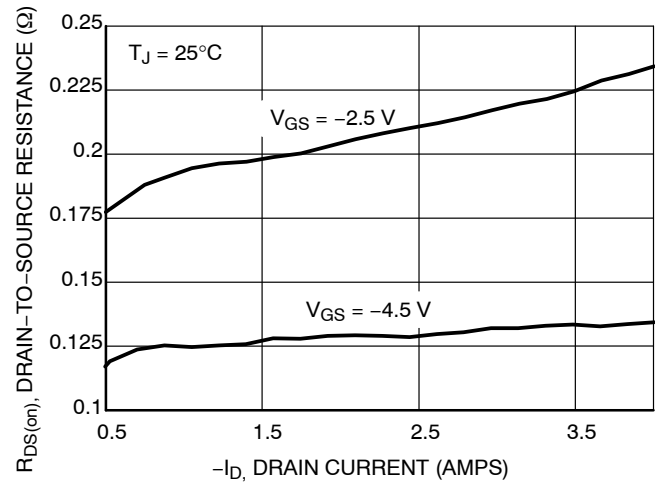


Figure 14. On-Resistance vs. Drain Current and Gate Voltage

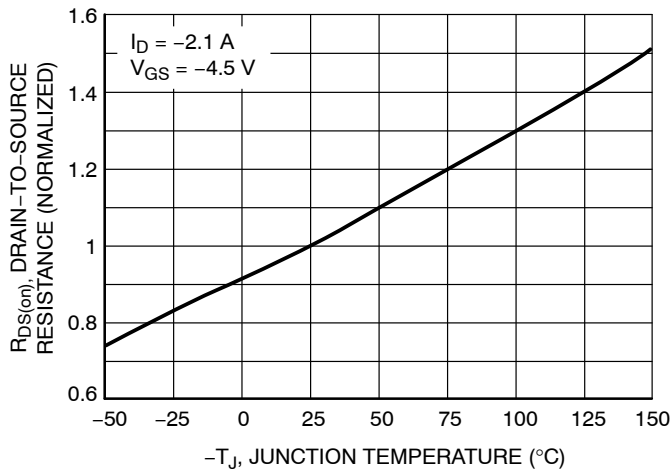


Figure 15. On-Resistance Variation with Temperature

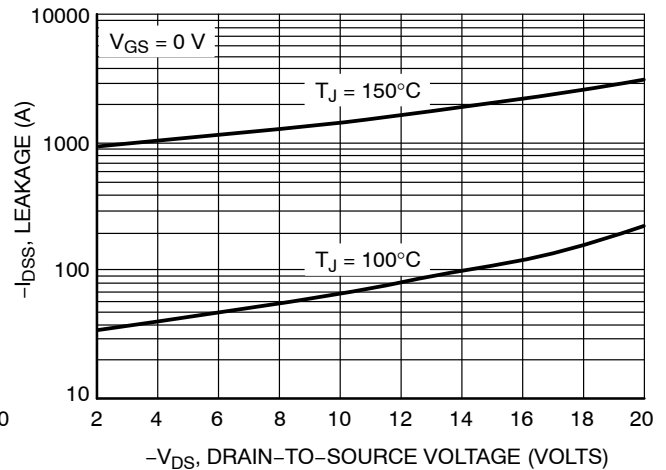


Figure 16. Drain-to-Source Leakage Current vs. Voltage

TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

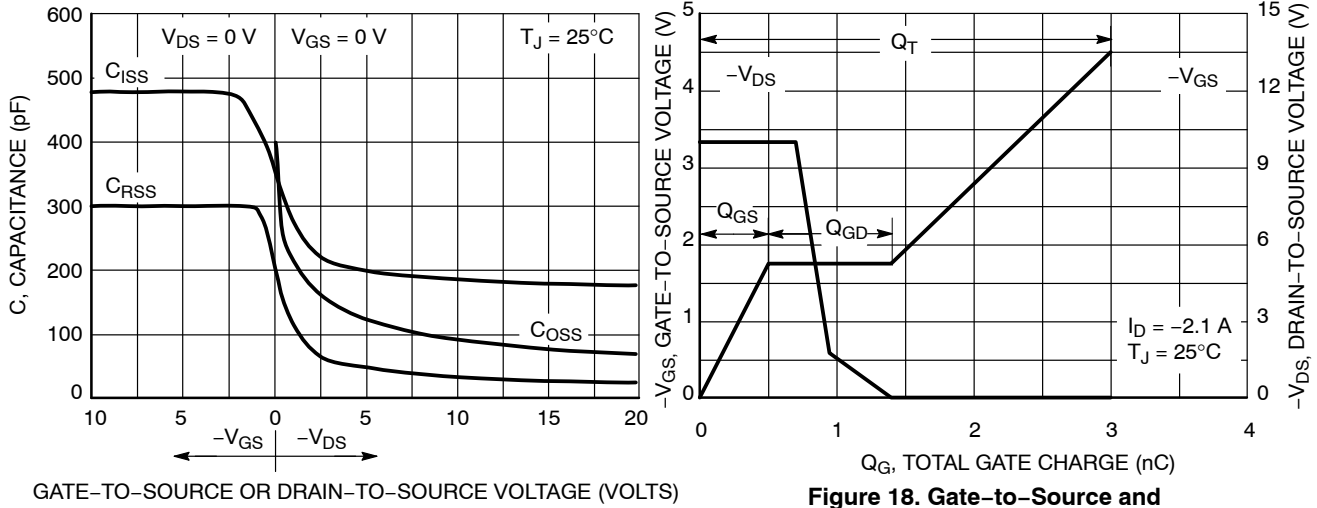


Figure 17. Capacitance Variation

Figure 18. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

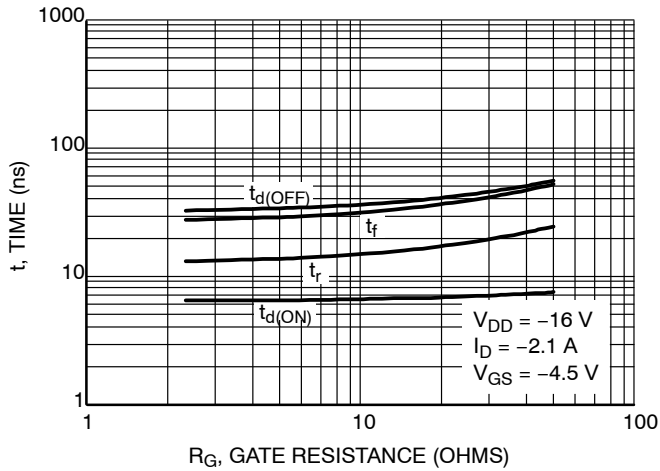


Figure 19. Resistive Switching Time Variation vs. Gate Resistance

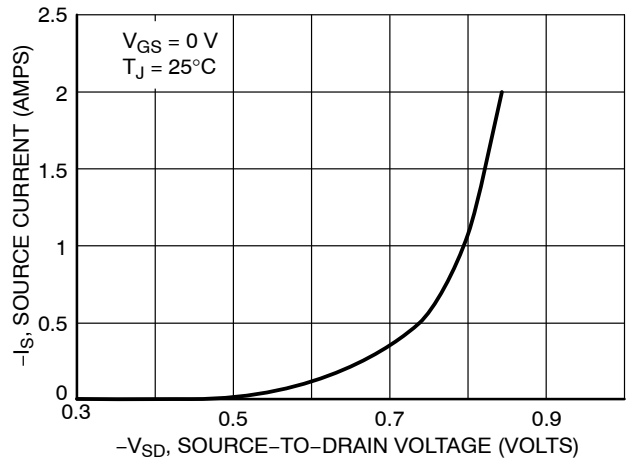


Figure 20. Diode Forward Voltage vs. Current

TYPICAL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

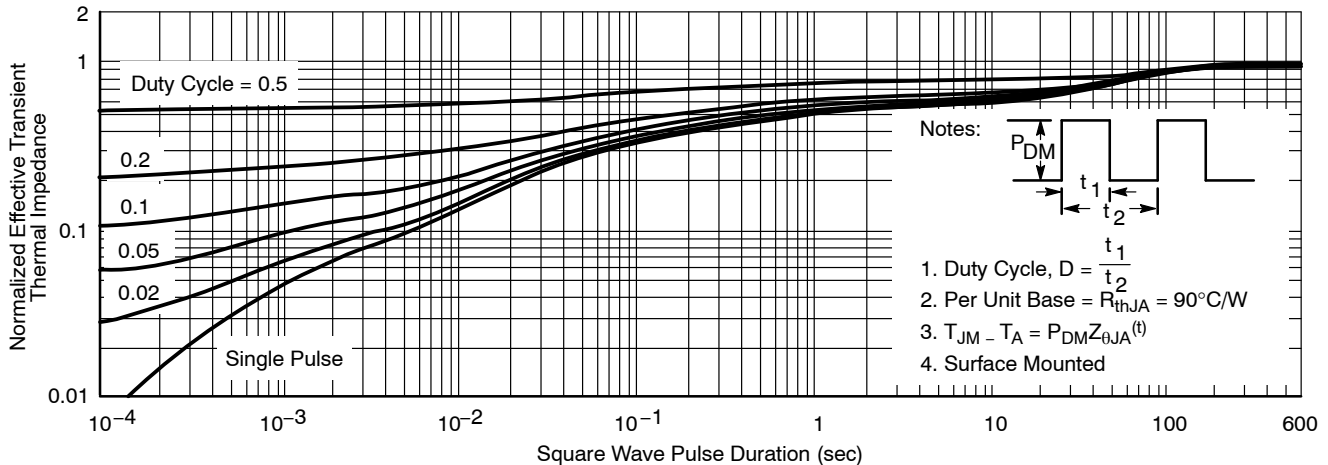


Figure 21. Thermal Response

SOLDERING FOOTPRINT*

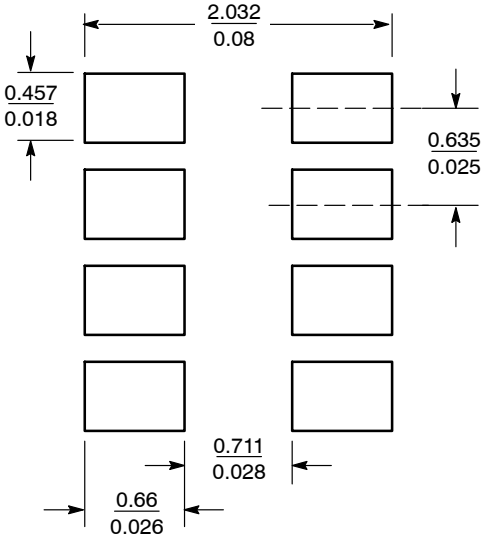


Figure 22. Basic

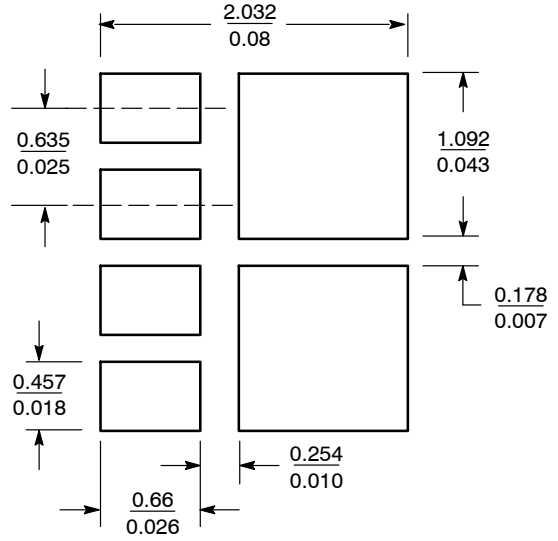


Figure 23. Style 2

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 22. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 23 improves the thermal area of the drain connections (pins 5, 6, 7, 8) while remaining within the

confines of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper lead-frame) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

MECHANICAL CASE OUTLINE

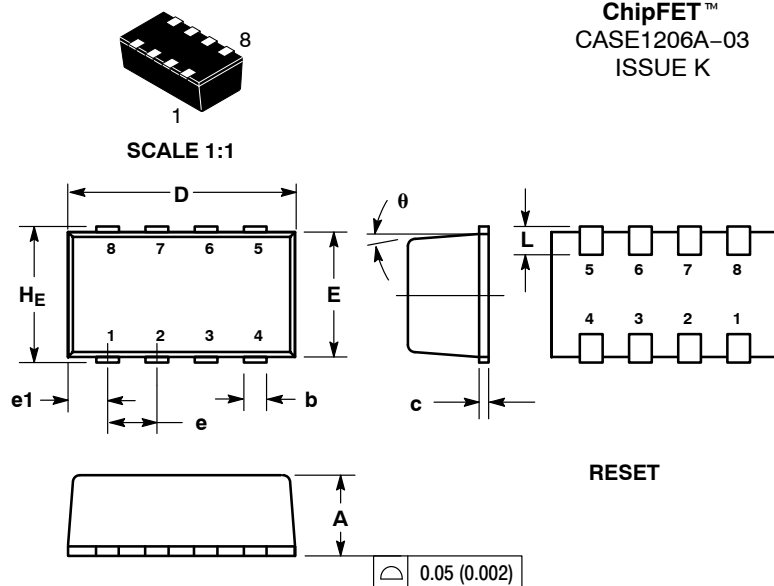
PACKAGE DIMENSIONS

ON Semiconductor®



ChipFET™
CASE1206A-03
ISSUE K

DATE 19 MAY 2009



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

STYLE 1:

- PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:

- PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:

- PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:

- PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

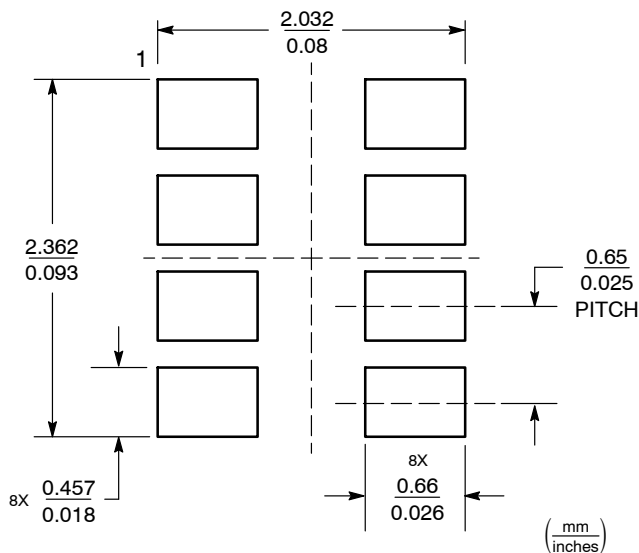
STYLE 5:

- PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

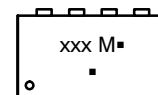
STYLE 6:

- PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- xxx = Specific Device Code
M = Month Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

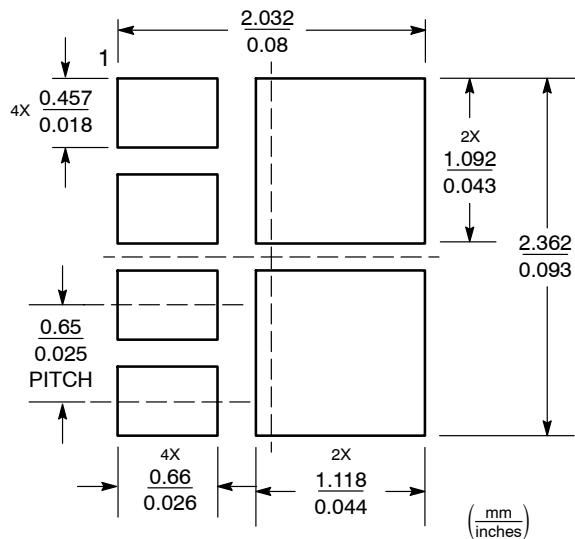
OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

DOCUMENT NUMBER:	98AON03078D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	ChipFET	PAGE 1 OF 2

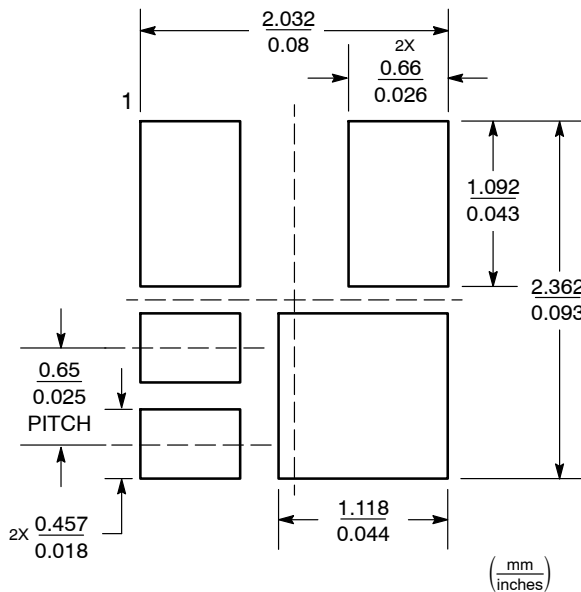
ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

Figure 1: Dimensions of the test specimen. The diagram shows a rectangular specimen with a central hole. Dimensions are given in inches and millimeters. The overall width is 2.032 inches (51.6 mm). The overall height is 1.727 inches (43.8 mm). The central hole has a diameter of 0.08 inches (2.0 mm). The distance from the top edge to the center of the hole is 2.362 inches (59.9 mm). The distance from the bottom edge to the center of the hole is 0.093 inches (2.4 mm). The distance from the left edge to the center of the hole is 0.457 inches (11.6 mm). The distance from the right edge to the center of the hole is 0.018 inches (0.5 mm). The distance from the center of the hole to the left edge of the hole is 0.66 inches (16.8 mm). The distance from the center of the hole to the right edge of the hole is 0.026 inches (0.7 mm).

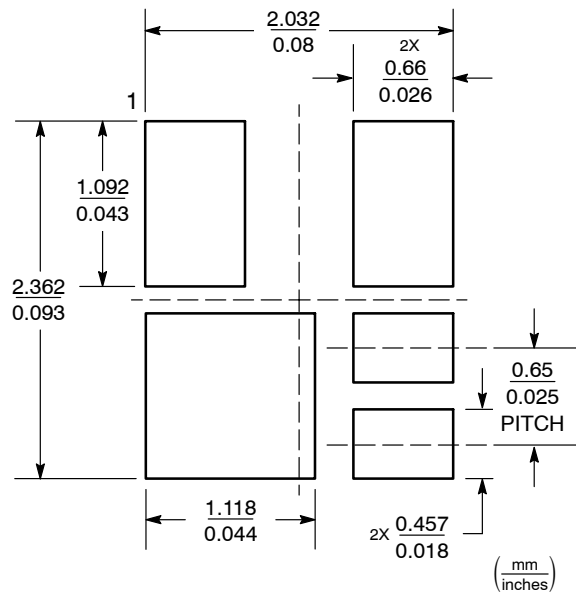
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON03078D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	ChipFET	PAGE 2 OF 2

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative