

Operational Amplifier, 36 V, 3 MHz, 0.95 mV Input Offset Voltage, Rail-to-Rail

NCS20231, NCV20231, NCS20232, NCV20232, NCS20234, NCV20234

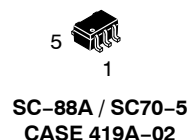
The NCS2023x series of op amps feature a wide supply range of 2.7 V to 36 V with an input offset voltage as low as ± 0.95 mV max. These op amps are available in single, dual, and quad channel configurations. Automotive qualified options are available under the NCV prefix with an optional extended operating temperature range from -40°C to 150°C . All other versions are specified over the operating temperature range from -40°C to 125°C .

Features

- Supply Voltage Range: 2.7 V to 36 V
- Temperature Range: -40°C to 150°C
- Unity Gain Bandwidth: 3 MHz
- Input Offset Voltage: ± 1.2 mV max, $T_A = -40$ to 150°C
- Input Offset Voltage Drift: ± 2 $\mu\text{V}/^{\circ}\text{C}$ max
- Common-Mode Input Voltage Range
 - ♦ Optimal: $V_{SS} - 0.1$ to $V_{DD} - 2$ V
 - ♦ Functional: $V_{SS} - 0.1$ to $V_{DD} + 0.1$ V
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Telecom Equipment
- Power Supply Designs
- Diesel Injection Control
- Automotive
- Motor Control



DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2 of this data sheet.

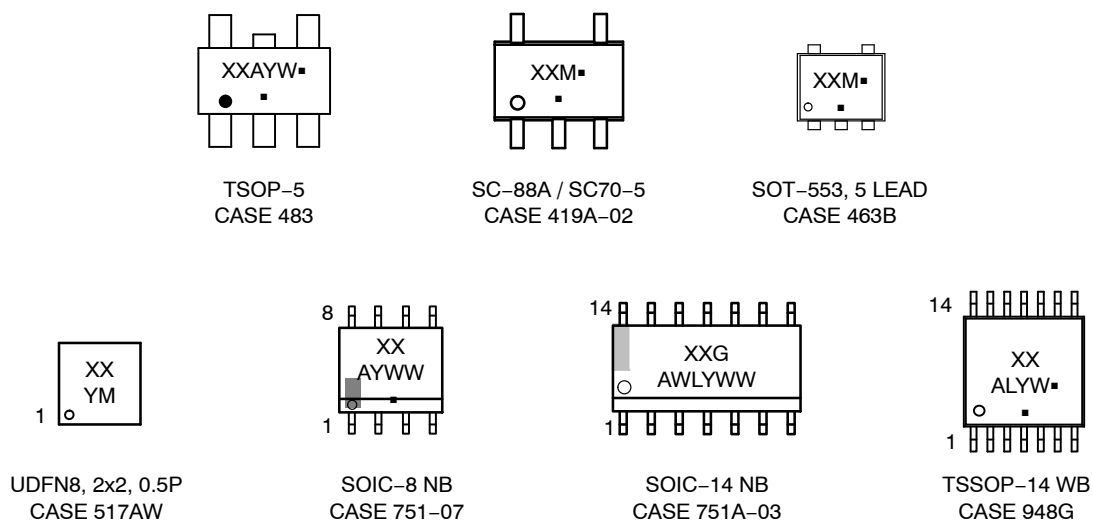
PIN CONNECTIONS

See pin connections on page 3 of this data sheet.

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

DEVICE MARKING INFORMATION



XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
M = Date Code
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

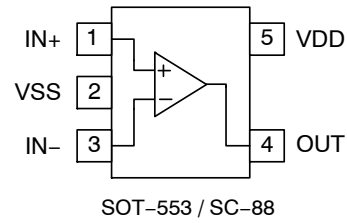
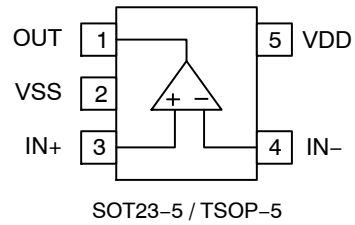
Temperature	Channels	Package	Device Part Number	Marking	Shipping [†]
Industrial and Commercial					
-40°C to 125°C	Single	TSOP-5	NCS20231SN2T1G	AAC	3000 / Tape & Reel
		SC-88	NCS20231SQ3T2G	AAG	3000 / Tape & Reel
		SOT-553	NCS20231XV53T2G	AC	4000 / Tape & Reel
	Dual	SOIC-8	NCS20232DR2G*	N232	2500 / Tape & Reel
		UDFN-8	NCS20232MUTBG*	DGA	3000 / Tape & Reel
	Quad	SOIC-14	NCS20234DR2G*	234G	2500 / Tape & Reel
TSSOP-14		NCS20234DTBR2G*	N234	2500 / Tape & Reel	
Automotive Qualified, Grade 1					
-40°C to 150°C	Single	TSOP-5	NCV20231SN2T1G	AAC	3000 / Tape & Reel
		SC-88	NCV20231SQ3T2G	AAG	3000 / Tape & Reel
		SOT-553	NCV20231XV53T2G	AC	4000 / Tape & Reel
	Dual	SOIC-8	NCV20232DR2G*	N232	2500 / Tape & Reel
	Quad	SOIC-14	NCV20234DR2G*	234G	2500 / Tape & Reel
		TSSOP-14	NCV20234DTBR2G*	N234	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

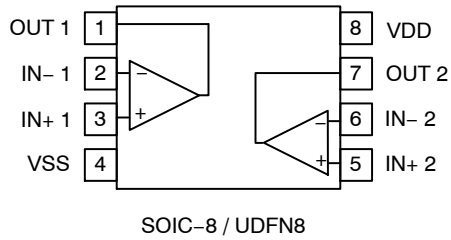
*In Development. Contact local sales office for more information.

PIN CONNECTIONS

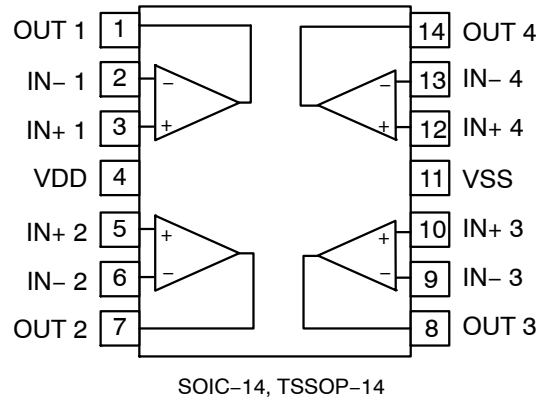
Single Channel



Dual Channel



Quad Channel



ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Supply Voltage Range ($V_{DD} - V_{SS}$)	V_S	-0.3 to 40	V
Input Common-Mode Voltage	V_{CM}	$V_{SS} - 0.2$ to $V_{DD} + 0.2$	V
Differential Input Voltage	V_{ID}	$\pm V_S$	V
Maximum Input Current	I_I	± 10	mA
Maximum Output Current	I_O	± 100	mA
Continuous Total Power Dissipation	P_D	200	mW
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
ESD Capability, Human Body Model (Note 2)	HBM	± 2000	V
ESD Capability, Charge Device Model (Note 2)	CDM	± 1000	V
Moisture Sensitivity Level	MSL	Level 1	
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area
2. This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per JEDEC standard JS-001-2017 (AEC-Q100-002)
ESD Charged Device Model tested per JEDEC standard JS-002-2014 (AEC-Q100-011)
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERM/D

THERMAL CHARACTERISTICS (Note 4)

Package	θ_{JA} Junction-to-Ambient Thermal Resistance	Ψ_{JT} Junction-to-Case Top Thermal Characteristic	Ψ_{JB} Junction-to-Board Thermal Characteristic	Unit
TSOP-5 / SOT23-5	254	78	150	°C/W
SC-88A / SC-70-5 / SOT-353	902	70	810	°C/W
SOT-553	238	14	134	°C/W
SOIC-8				°C/W
UDFN-8				°C/W
SOIC-14				°C/W
TSSOP-14				°C/W

4. Thermal parameters are based on a 2s2p board following JESD51-7 (JEDEC)

RECOMMENDED OPERATING RANGES (Note 5)

Parameter	Symbol	Min	Max	Unit
Supply Voltage ($V_{DD} - V_{SS}$)	V_S	2.7	36	V
Differential Input Voltage ($V_{IN+} - V_{IN-}$)	V_{ID}		± 5 (Note 6)	V
Input Common-Mode Range (Note 7)	V_{CM}	$V_{SS} - 0.1$	$V_{DD} - 2$ V	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area
6. The differential voltage may not exceed the supply voltage, $\pm V_S$. For supplies greater than $V_S = 5$ V, differential voltages up to $\pm V_S$ will consume more input current. See APPLICATION INFORMATION.
7. The specified input common mode range yields the best performance. However, the input common mode range is functional up to $V_{DD} + 0.1$ V. See APPLICATION INFORMATION.

NCS20231, NCV20231, NCS20232, NCV20232, NCS20234, NCV20234

ELECTRICAL CHARACTERISTICS ($V_S = 2.7\text{ V to }36\text{ V}$)

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

Boldface limits apply over the specified temperature range, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Supply Voltage (V)	Temp ($^\circ\text{C}$)	Min	Typ	Max	Unit
INPUT CHARACTERISTICS								
Offset Voltage	V_{OS}	$V_{CM} = \text{mid-supply}$	2.7, 5, 10, 36	25		± 0.3	± 0.95	mV
				-40 to 125			± 1.2	
				-40 to 150			± 1.2	
Offset Voltage Drift over Temperature	dV_{OS}/dT	$V_{CM} = \text{mid-supply}$	2.7, 5, 10, 36	-40 to 125		± 0.5	± 2	$\mu\text{V}/^\circ\text{C}$
				-40 to 150		± 0.5	± 5	
Input Bias Current (Note 8)	I_{IB}		2.7, 5, 10, 36	25		± 5	± 60	pA
				-40 to 125			± 3000	
				150		± 10000		
Input Offset Current (Note 8)	I_{OS}		2.7	25		± 0.5	± 60	pA
				-40 to 125			± 500	
				-40 to 150			± 2000	
			5, 10	25		± 0.5	± 60	
				-40 to 125			± 800	
				-40 to 150			± 2500	
			36	25		± 0.5	± 60	pA
				-40 to 125			± 2000	
				-40 to 150			± 2500	
Channel Separation		NCS20232, NCS20234	2.7, 5, 10, 36	25		130		dB
Input Capacitance	C_{IN}	IN+	2.7, 36	25		1		pF
		IN-	2.7, 36	25		6		
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{SS} - 0.1\text{ V to }V_{DD} - 2\text{ V}$	2.7	25	80	98		dB
				-40 to 125	75			
				-40 to 150	69			
			5 (Note 8)	25	90	105		
				-40 to 125	85			
				-40 to 150	80			
			10 (Note 8)	25	100	117		
				-40 to 125	100			
				-40 to 150	94			
			36	25	110	122		
				-40 to 125	110			
				-40 to 150	107			
		$V_{CM} = V_{SS} + 1.8\text{ V to }V_{DD} - 2.4\text{ V}$	36	25	117 (Note 8)	125		dB
EMI Rejection Ratio	EMIRR		2.7, 36	25		See Figure 29		dB

8. Guaranteed by design and/or characterization.

NCS20231, NCV20231, NCS20232, NCV20232, NCS20234, NCV20234

ELECTRICAL CHARACTERISTICS ($V_S = 2.7\text{ V to }36\text{ V}$) (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

Boldface limits apply over the specified temperature range, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Supply Voltage (V)	Temp ($^\circ\text{C}$)	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS								
Open Loop Voltage Gain	A_{VOL}	$V_{CM} = \text{mid-supply}$	2.7	25	100	115		dB
				-40 to 125	90			
				-40 to 150	90			
			5 (Note 9)	25	120	135		
				-40 to 125	115			
				-40 to 150	115			
			10 (Note 9)	25	130	145		
				-40 to 125	120			
				-40 to 150	120			
			36	25	135	154		
				-40 to 125	130			
				-40 to 150	130			
Open Loop Output Impedance	Z_{OUT}					See Figure 28		Ω
High Level Output Voltage Swing from V_{DD}	$V_{DD}-V_{OH}$	$R_L = 10\text{ k}\Omega$	2.7, 5, 10, 36	25		60	80	mV
				-40 to 125			120	
				-40 to 150			150	
		$R_L = 1\text{ mA}$	2.7, 5, 10, 36	25		40	60	
				-40 to 125			80	
				-40 to 150			100	
		$R_L = 5\text{ mA}$	10	25		165	200	
				-40 to 125			350	
				-40 to 150			400	
Low Level Output Voltage Swing from V_{SS}	$V_{OL}-V_{SS}$	$R_L = 10\text{ k}\Omega$	2.7, 5, 10	25		16	30	mV
				-40 to 125			50	
				-40 to 150			50	
			36	25		55	80	
				-40 to 125			250	
				-40 to 150			120	
		$R_L = 1\text{ mA}$	2.7, 5, 10, 36	25		35	50	
				-40 to 125			80	
				-40 to 150			80	
		$R_L = 5\text{ mA}$	10	25		150	170	
				-40 to 125			300	
				-40 to 150			300	
Output Current Capability	I_{OUT}	Output to V_{DD} rail, sinking current	2.7, 5, 10, 36	25		28		mA
		Output to V_{SS} rail, sourcing current	2.7, 5, 10, 36	25		28		
Capacitive Load Drive	C_L	Phase margin = 35°	2.7 to 36	25		140		pF

9. Guaranteed by design and/or characterization.

NCS20231, NCV20231, NCS20232, NCV20232, NCS20234, NCV20234

ELECTRICAL CHARACTERISTICS ($V_S = 2.7\text{ V to }36\text{ V}$) (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

Boldface limits apply over the specified temperature range, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Supply Voltage (V)	Temp ($^\circ\text{C}$)	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE								
Gain Bandwidth Product	GWBP	$C_L = 25\text{ pF}$	2.7, 5, 10, 36	25		3		MHz
Gain Margin	A_m	$C_L = 25\text{ pF}$	2.7, 5, 10, 36	25		16		dB
Phase Margin	Φ_m	$C_L = 25\text{ pF}$	2.7, 5, 10, 36	25		60		$^\circ$
Slew Rate	SR	Unity gain, $R_L = 2\text{ k}\Omega$	2.7, 5, 10, 36	25		4		V/ μs
Settling Time to 0.1 %	t_s	$V_{IN} = 1\text{ V step}$	2.7	25		7		μs
		$V_{IN} = 3\text{ V step}$	5	25		7		
		$V_{IN} = 8\text{ V step}$	10	25		7		
		$V_{IN} = 10\text{ V step}$	36	25		6		
Settling Time to 0.01 %	t_s	$V_{IN} = 1\text{ V step}$	2.7	25		20		μs
		$V_{IN} = 3\text{ V step}$	5	25		10		
		$V_{IN} = 8\text{ V step}$	10	25		9		
		$V_{IN} = 10\text{ V step}$	36	25		9		

NOISE PERFORMANCE

Total Harmonic Distortion + Noise	THD+ N	$V_{IN} = 0.5\text{ V}_{pp}$, $f = 1\text{ kHz}$, $A_V = 1$	2.7	25		0.009		%
		$V_{IN} = 2.5\text{ V}_{pp}$, $f = 1\text{ kHz}$, $A_V = 1$	5	25		0.0004		
		$V_{IN} = 7.5\text{ V}_{pp}$, $f = 1\text{ kHz}$, $A_V = 1$	10	25		0.0002		
		$V_{IN} = 28.5\text{ V}_{pp}$, $f = 1\text{ kHz}$, $A_V = 1$	36	25		0.0002		
Voltage Noise Density	e_n	$f = 1\text{ kHz}$	2.7, 5, 10, 36	25		20		nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$				20		
Current Noise Density	i_n	$f = 1\text{ kHz}$	2.7, 5, 10, 36	25		30		fA/ $\sqrt{\text{Hz}}$
Voltage Noise, Peak to Peak	e_{pp}	$f_{IN} = 0.1\text{ Hz to }10\text{ Hz}$	2.7, 5, 10, 36	25		700		nV $_{pp}$

POWER SUPPLY

Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to }36\text{ V}$	2.7, 36	25	125	138		dB
				-40 to 125	120			
				-40 to 150	120			
Quiescent Current	I_Q	No load, per channel	2.7, 5	25		0.37	0.595	mA
				-40 to 125			0.650	
				-40 to 150			0.7	
			10	25		0.375	0.595	
				-40 to 125			0.650	
				-40 to 150			0.75	
			36	25		0.41	0.595	
				-40 to 125			0.650	
				-40 to 150			0.8	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

Typical Performance at $T_A = 25^\circ\text{C}$, $V_{CM} = \text{mid-supply}$, $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ to mid-supply, unless otherwise noted

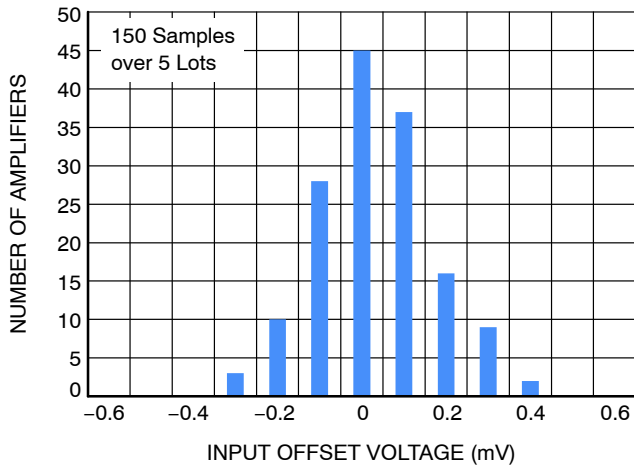


Figure 1. Input Offset Voltage Distribution

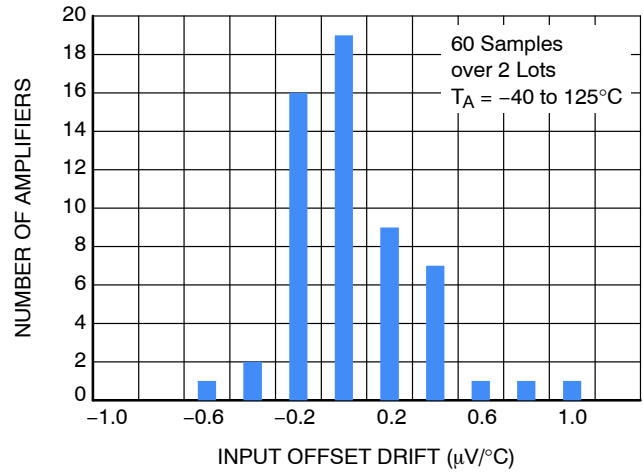


Figure 2. Input Offset Voltage Drift Distribution

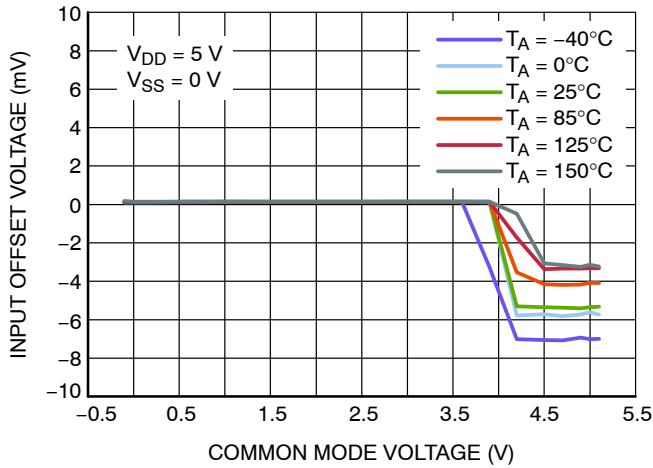


Figure 3. Input Offset Voltage vs. Common Mode Voltage

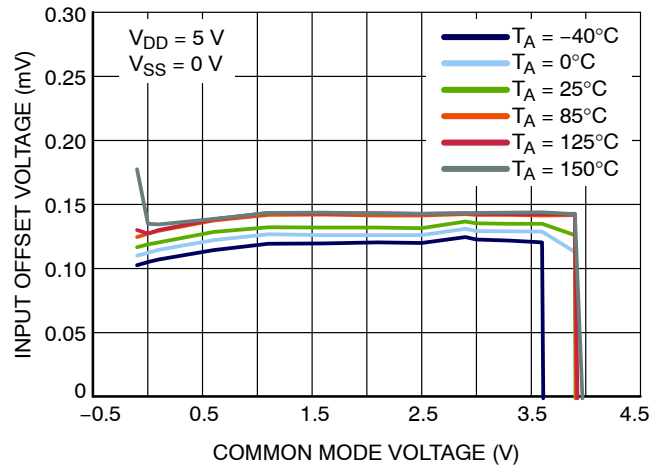


Figure 4. Input Offset Voltage vs. Common Mode Voltage, Performance Region

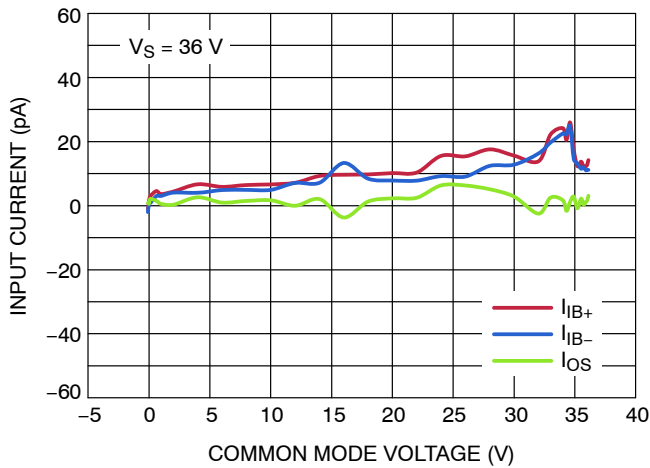


Figure 5. Input Current vs. Common Mode Voltage

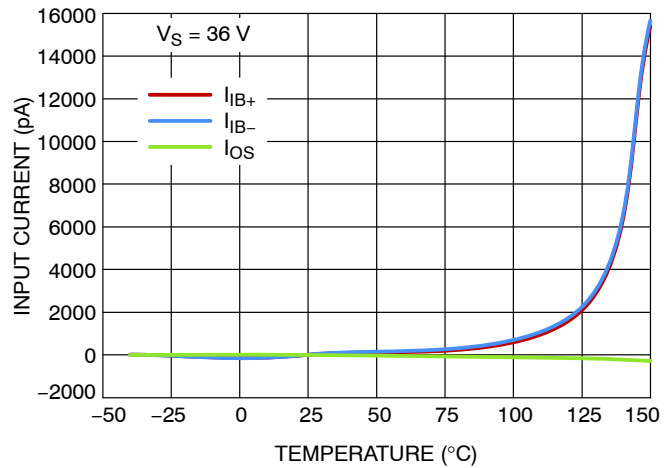


Figure 6. Input Current vs. Temperature

TYPICAL CHARACTERISTICS

Typical Performance at $T_A = 25^\circ\text{C}$, $V_{CM} = \text{mid-supply}$, $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ to mid-supply, unless otherwise noted

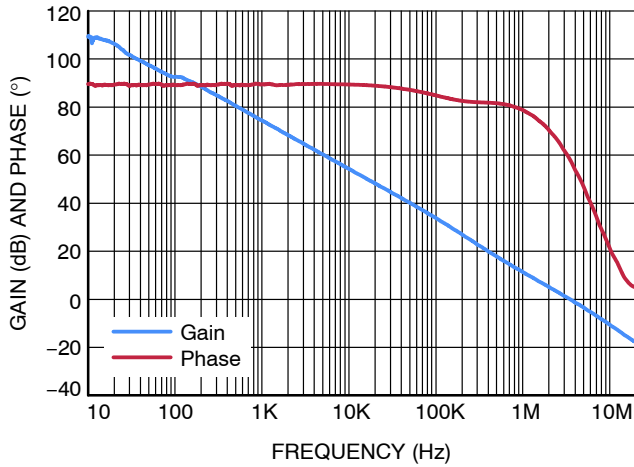


Figure 7. Open Loop Gain and Phase vs. Frequency

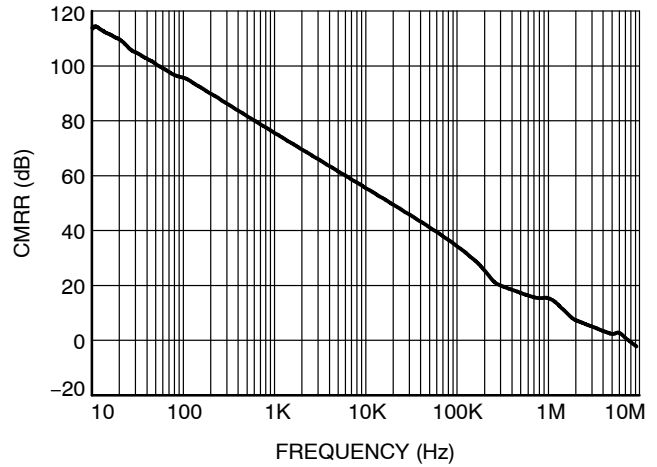


Figure 8. CMRR vs. Frequency

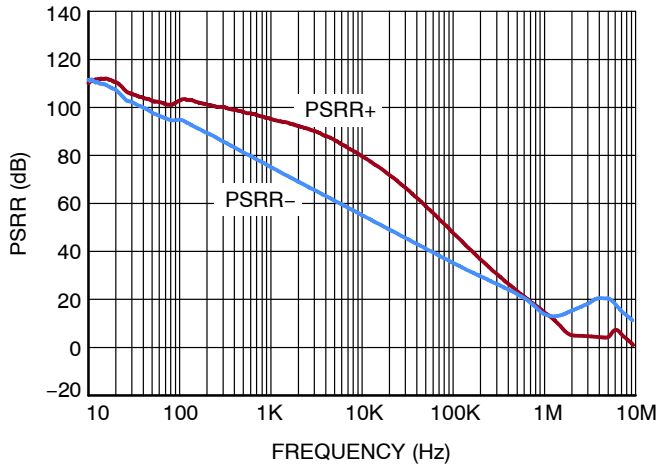


Figure 9. PSRR vs. Frequency

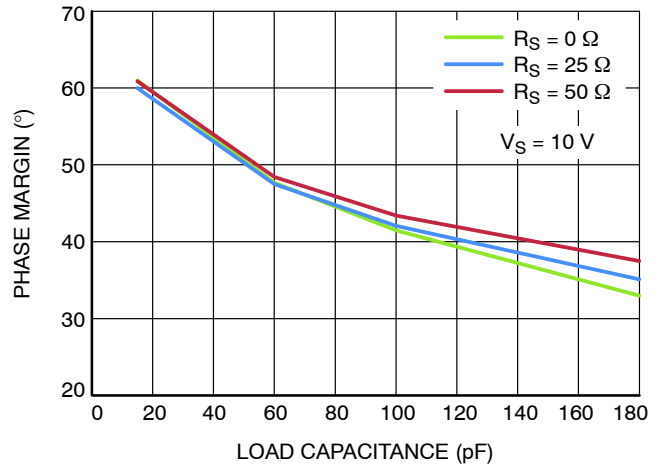


Figure 10. Phase Margin vs. Capacitive Load

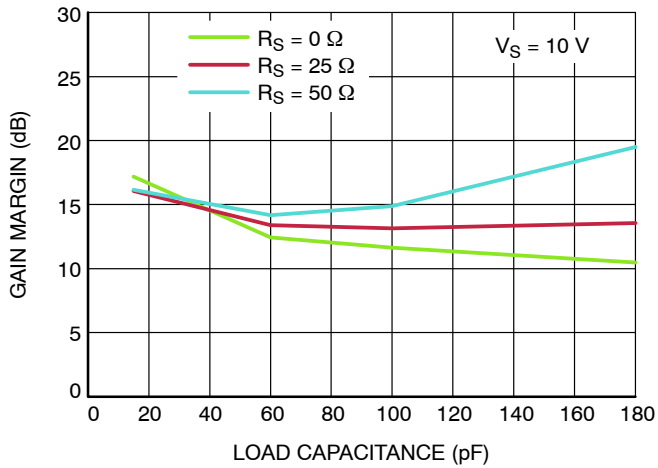


Figure 11. Gain Margin vs. Capacitive Load

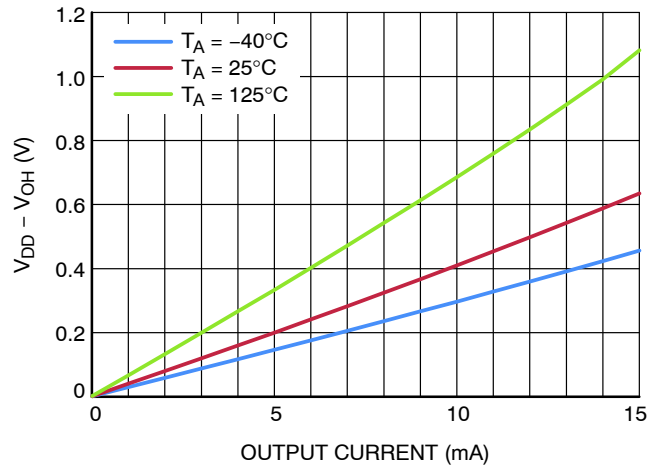


Figure 12. Output Voltage Swing High vs. Output Current at $V_S = 2.7\text{ V}$

TYPICAL CHARACTERISTICS

Typical Performance at $T_A = 25^\circ\text{C}$, $V_{CM} = \text{mid-supply}$, $C_L = 20 \text{ pF}$, $R_L = 10 \text{ k}\Omega$ to mid-supply, unless otherwise noted

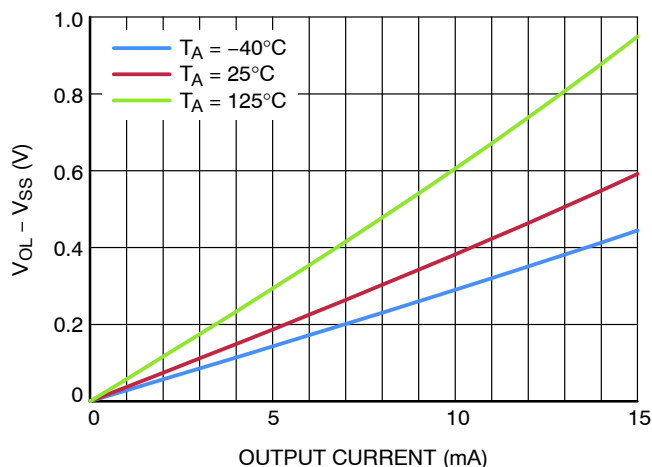


Figure 13. Output Voltage Swing vs. Output Current at $V_S = 2.7 \text{ V}$

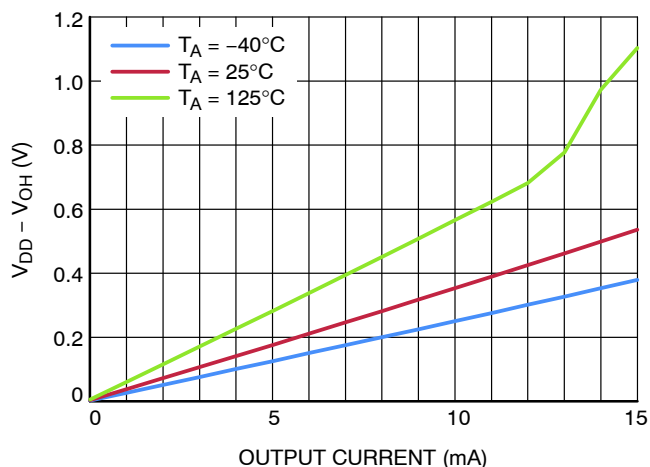


Figure 14. Output Voltage Swing vs. Output Current at $V_S = 36 \text{ V}$

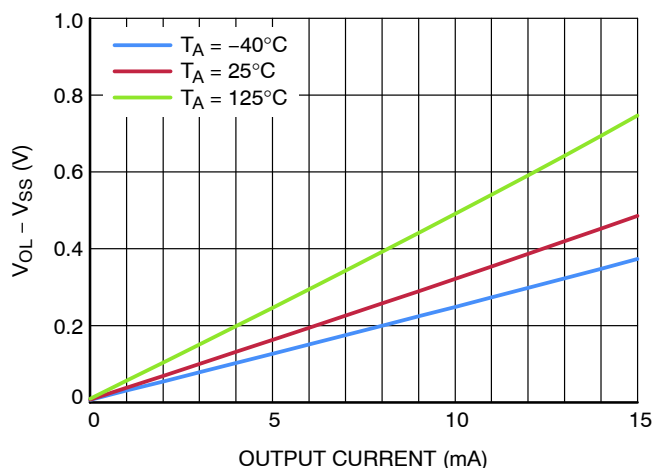


Figure 15. Output Voltage Swing vs. Output Current at $V_S = 36 \text{ V}$

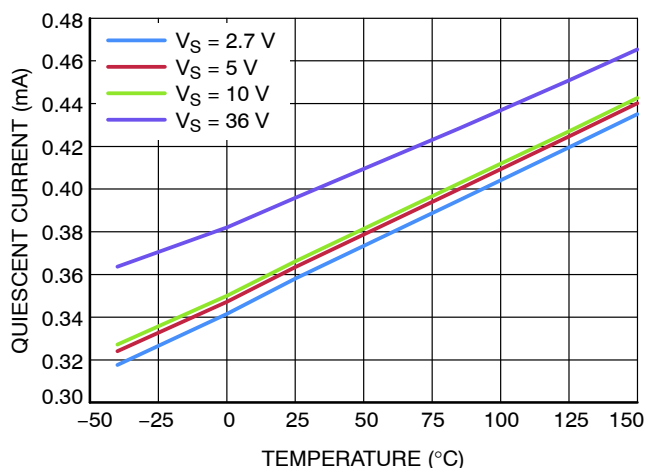


Figure 16. Quiescent Current vs. Temperature

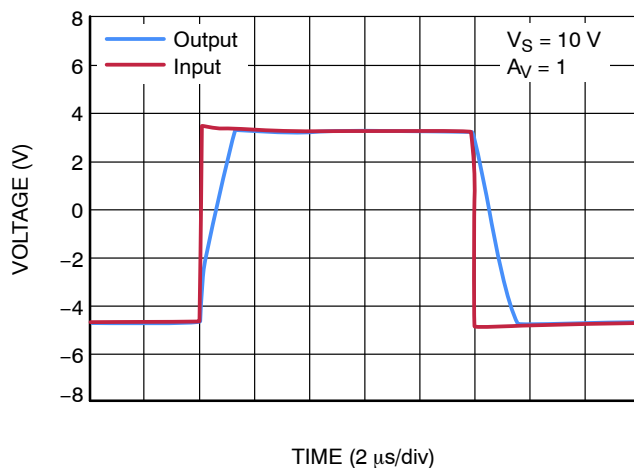


Figure 17. Large Signal Step Response

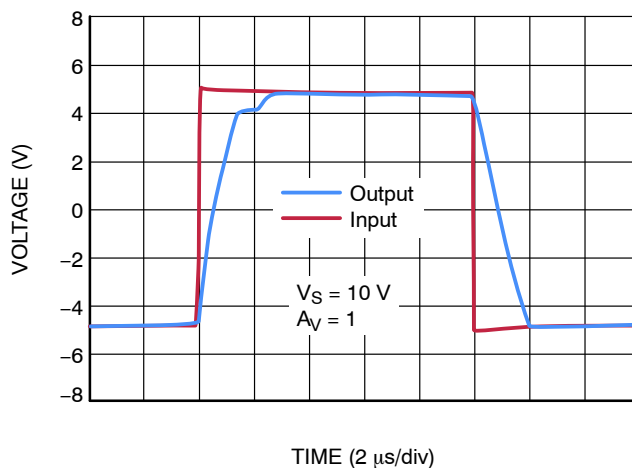
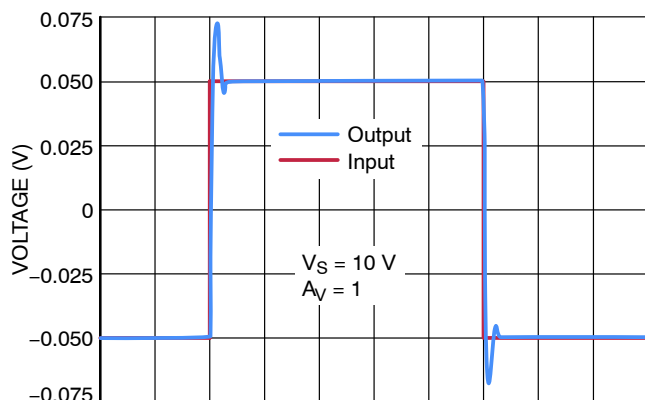


Figure 18. Large Signal Step Response

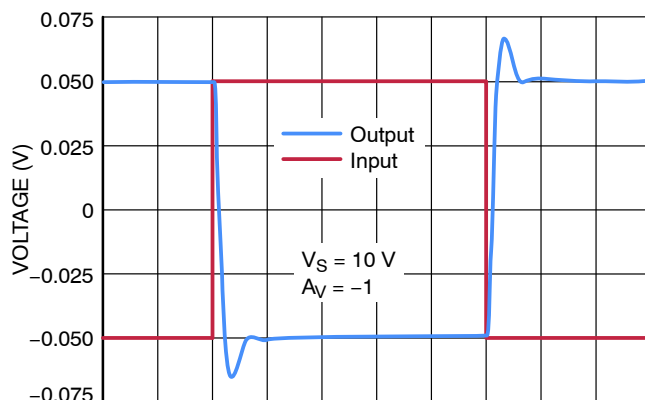
TYPICAL CHARACTERISTICS

Typical Performance at $T_A = 25^\circ\text{C}$, $V_{CM} = \text{mid-supply}$, $C_L = 20 \text{ pF}$, $R_L = 10 \text{ k}\Omega$ to mid-supply, unless otherwise noted



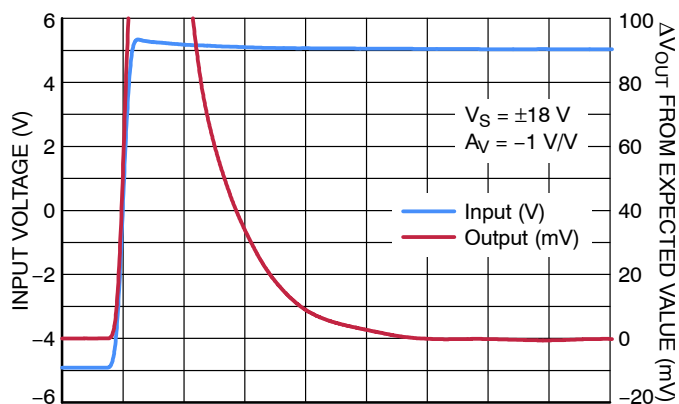
TIME (1 $\mu\text{s}/\text{div}$)

Figure 19. Small Signal Step Response



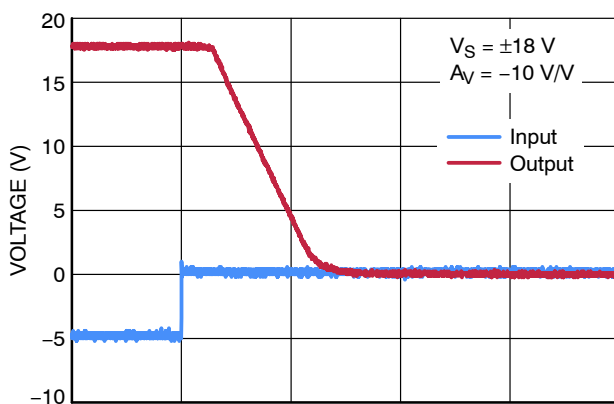
TIME (1 $\mu\text{s}/\text{div}$)

Figure 20. Small Signal Step Response



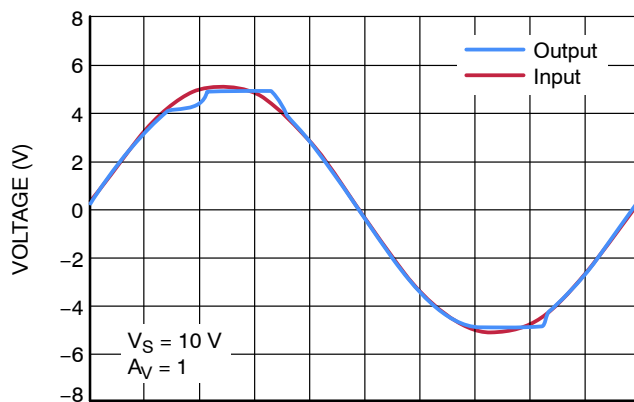
TIME (2 $\mu\text{s}/\text{div}$)

Figure 21. Settling Time



TIME (4 $\mu\text{s}/\text{div}$)

Figure 22. Output Overload Recovery Response



TIME (2 $\mu\text{s}/\text{div}$)

Figure 23. No Phase Reversal

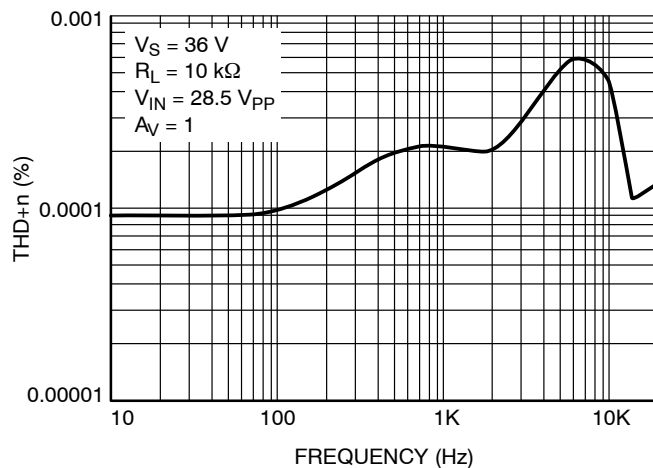


Figure 24. THD+n vs. Frequency

TYPICAL CHARACTERISTICS

Typical Performance at $T_A = 25^\circ\text{C}$, $V_{CM} = \text{mid-supply}$, $C_L = 20 \text{ pF}$, $R_L = 10 \text{ k}\Omega$ to mid-supply, unless otherwise noted

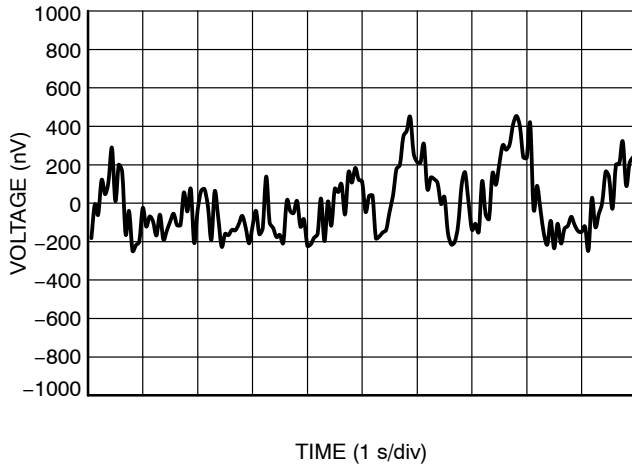


Figure 25. 0.1 Hz to 10 Hz Noise

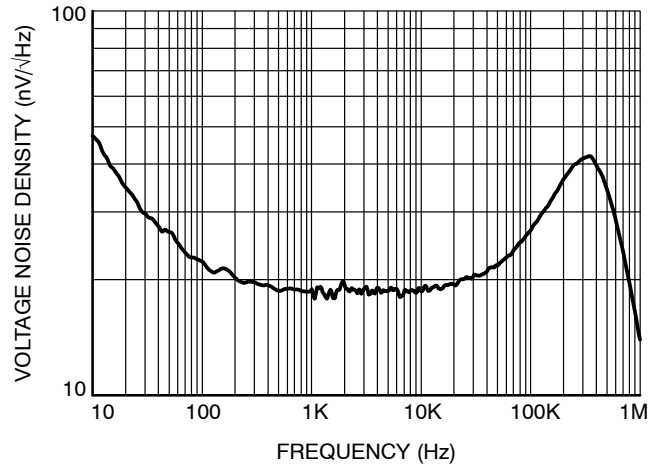


Figure 26. Voltage Noise Density vs. Frequency

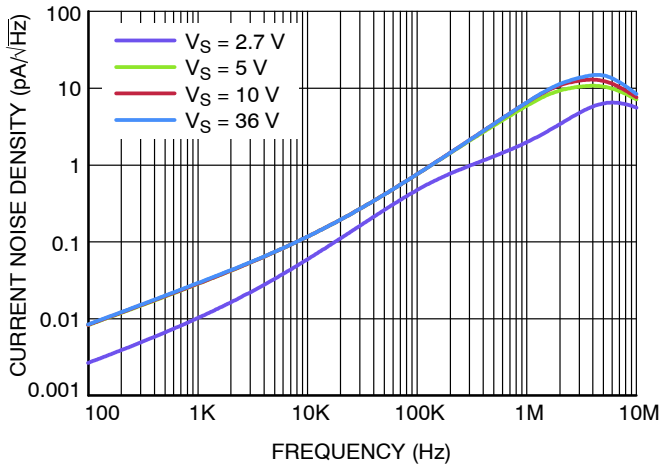


Figure 27. Current Noise Density vs. Frequency

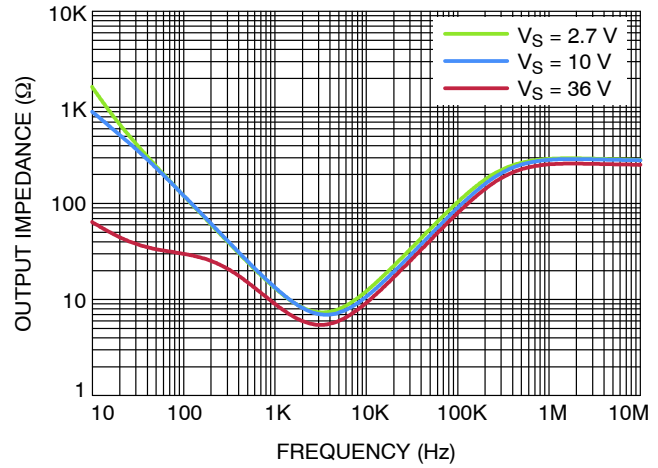


Figure 28. Open Loop Output Impedance vs. Frequency

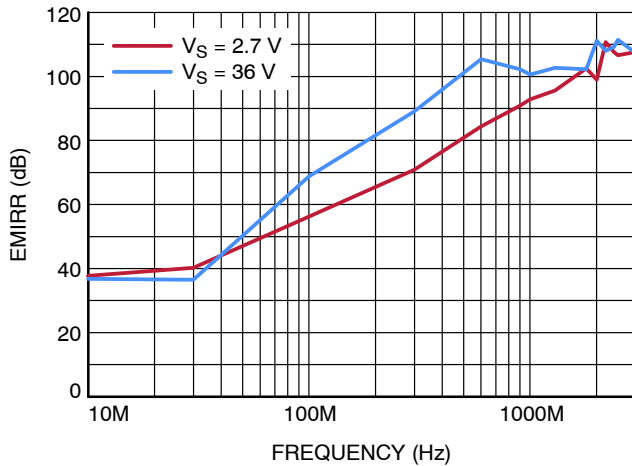


Figure 29. EMIRR vs. Frequency

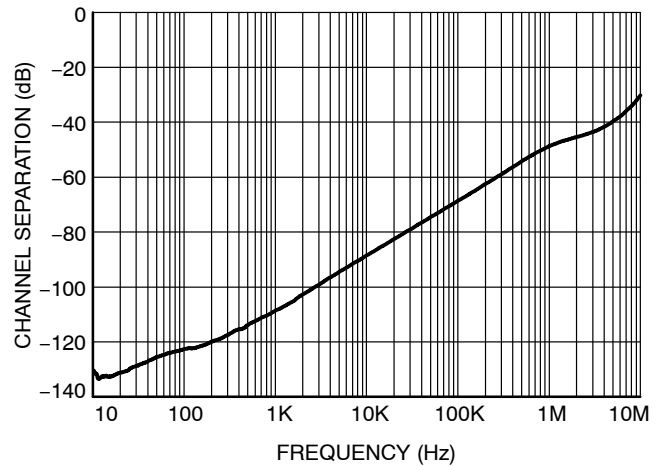


Figure 30. Channel Separation vs. Frequency

APPLICATION INFORMATION

Input and ESD Structure

The NCS20231 series amplifiers have back-to-back Zener diodes, which allow for normal operation with the differential voltage up to ± 5 V. Differential voltages beyond this are permitted, up to $\pm V_S$, but increased input leakage

current should be expected. Internal current limiting resistors in series with the input pins limit the current to ± 10 mA in scenarios where the differential voltage is as high as ± 36 V.

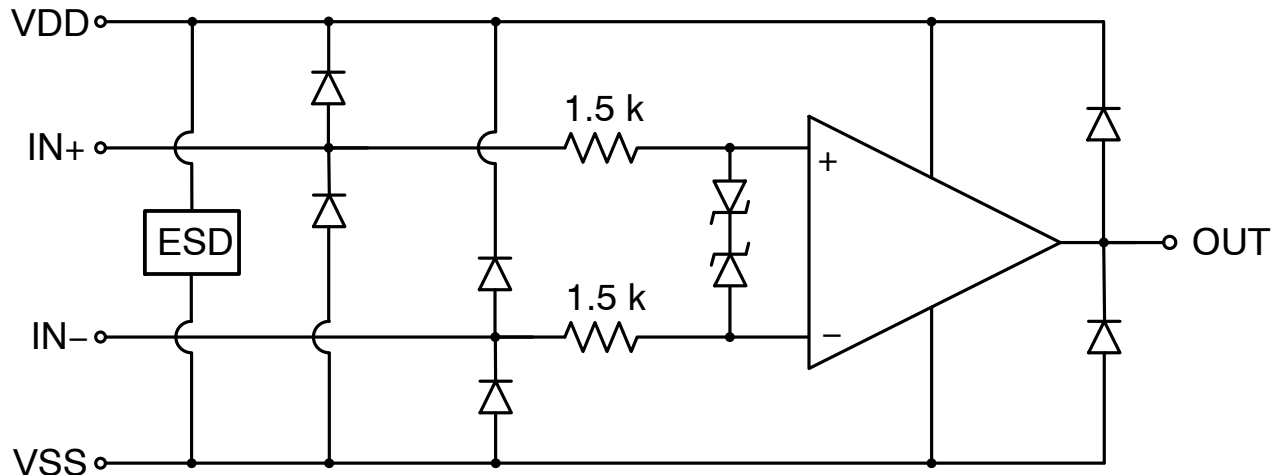


Figure 31. Representative Schematic of the Op Amp

Each input pin is diode clamped to the rails. In case of an input overvoltage, input currents must be limited to within ± 10 mA to prevent excessive current from damaging the part.

Rail-to-Rail Performance

The functional common mode input voltage spans 100 mV beyond the rails. High precision performance, as

shown throughout the ELECTRICAL CHARACTERISTICS table, is achieved in the $V_{SS} - 0.1$ V to $V_{DD} - 2$ V common mode voltage range. The input common mode extends further up to $V_{DD} + 0.1$ V to ensure functionality near the upper rail, though without precision performance in that region. The typical performance within the $V_{DD} - 2$ V to $V_{DD} + 0.1$ V range is shown in the table below.

Parameter	Symbol	Conditions	Typ	Units
Input Offset Voltage	V_{OS}	$V_{CM} = V_{DD} - 0.5$ V	± 9	mV
Input Offset Voltage over Temperature	dV_{OS}/dT		± 24	$\mu V/^{\circ}C$
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{DD} - 0.5$ V to $V_{DD} + 0.1$ V	75	dB
Open Loop Voltage Gain	A_{VOL}	$V_{CM} = V_{DD} - 0.5$ V	90	dB
Gain Bandwidth Product	GBWP	$V_{CM} = V_{DD} - 0.5$ V, $C_L = 25$ pF	2.5	MHz
Slew Rate	SR	Unity gain, $V_{CM} = V_{DD} - 1$ V to $V_{DD} - 0.2$ V	1.2	V/ μs
Voltage Noise Density	e_n	$f = 1$ kHz	1000	nV/ $\sqrt{Hz}$

The NCS2023x does not exhibit output phase reversal. Phase reversal occurs in some amplifiers when the input voltage exceeds the recommended input common mode voltage range, causing the output to flip to the opposite rail.

Instead, when the input common mode voltage range is exceeded on the NCS2023x, the output becomes clipped at the output, limited by the output voltage swing.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

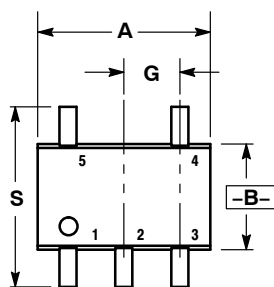
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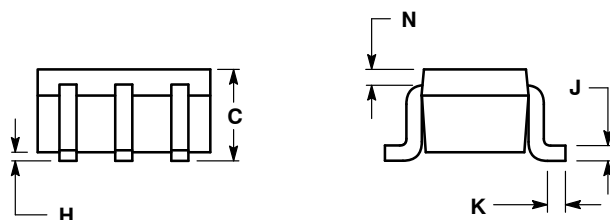
SCALE 2:1

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE L

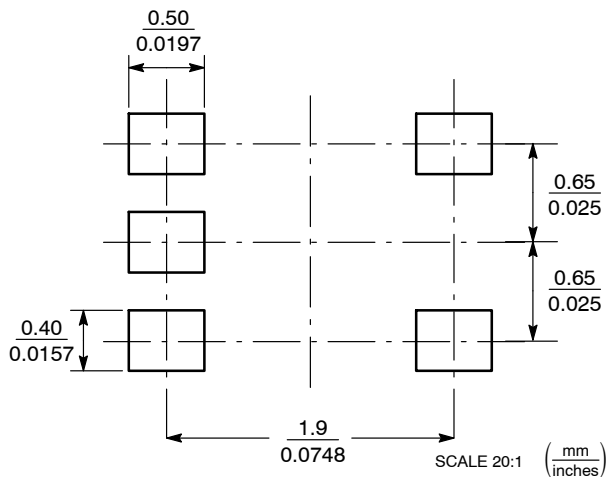
DATE 17 JAN 2013



D 5 PL $\oplus$ 0.2 (0.008) (M) B (M)



SOLDER FOOTPRINT



STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

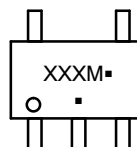
Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- 419A-01 OBSOLETE. NEW STANDARD 419A-02.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION: SC-88A (SC-70-5/SOT-353)

PAGE 1 OF 1

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



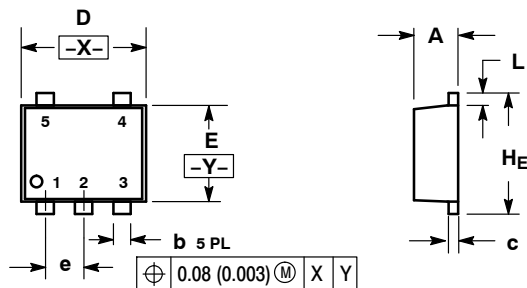
SCALE 4:1

SOT-553, 5 LEAD

CASE 463B

ISSUE C

DATE 20 MAR 2013

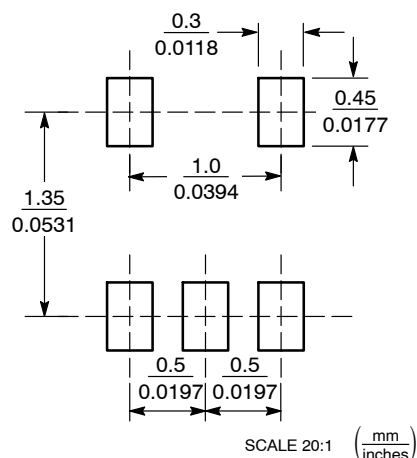


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.55	1.60	1.65	0.061	0.063	0.065

RECOMMENDED SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
M = Date Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:

- PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:

- PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 3:

- PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:

- PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 6:

- PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR 1
5. COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:

- PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

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NEW STANDARD:		
DESCRIPTION:	SOT-553, 5 LEAD	PAGE 1 OF 2

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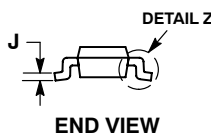
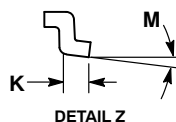
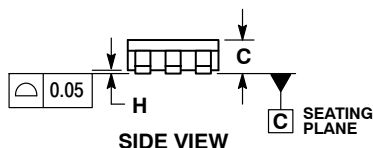
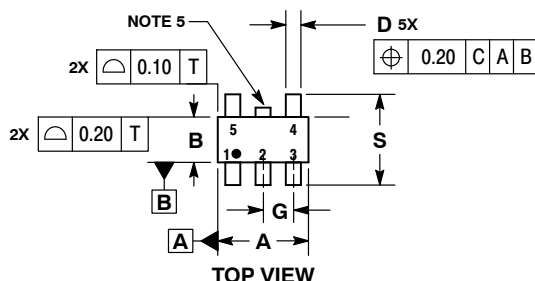
ON Semiconductor®



SCALE 2:1

TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020

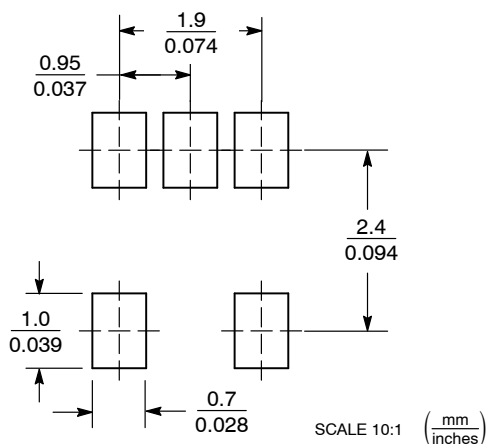


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

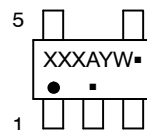
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	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

SOLDERING FOOTPRINT*

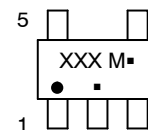


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION: TSOP-5

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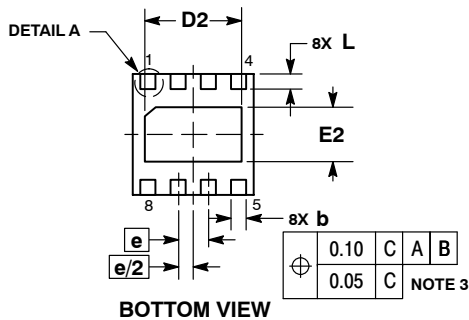
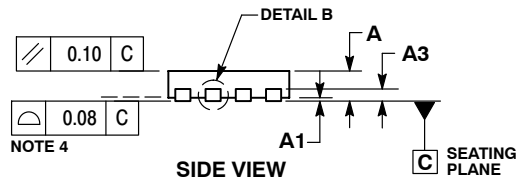
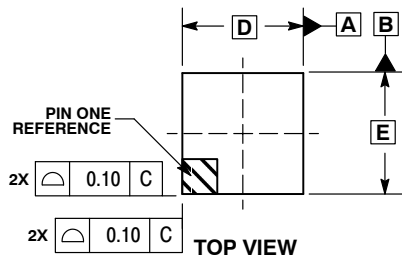
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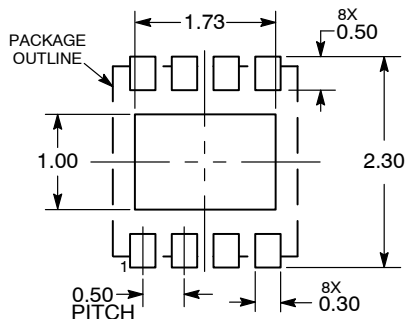
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UDFN8, 2x2 CASE 517AW ISSUE A

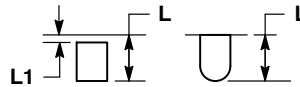
DATE 13 NOV 2015



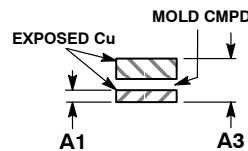
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS



DETAIL A
ALTERNATE
CONSTRUCTIONS



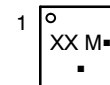
DETAIL B
ALTERNATE
CONSTRUCTION

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.18	0.30
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.50 BSC	
L	0.20	0.45
L1	---	0.15

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	UDFN8, 2X2	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

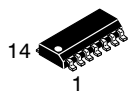
DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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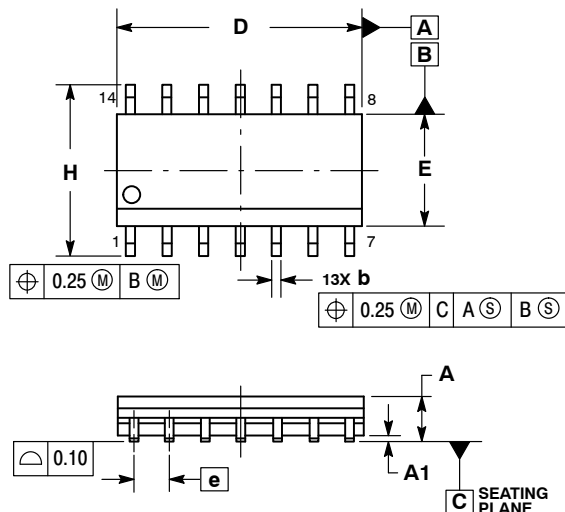
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

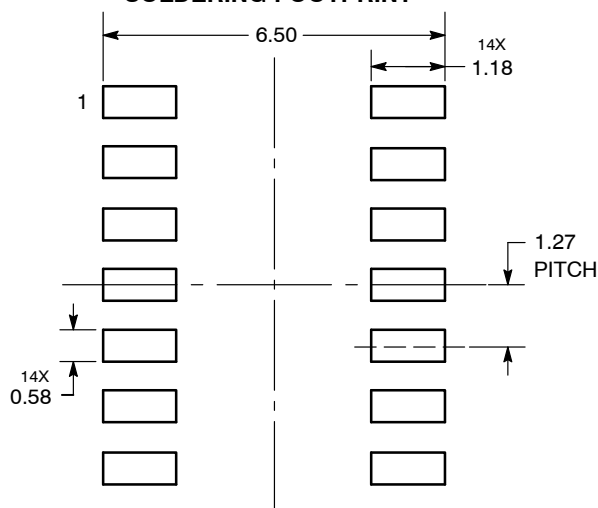


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

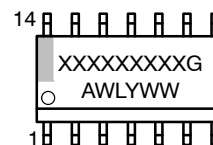
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

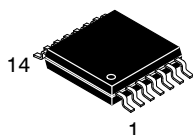
STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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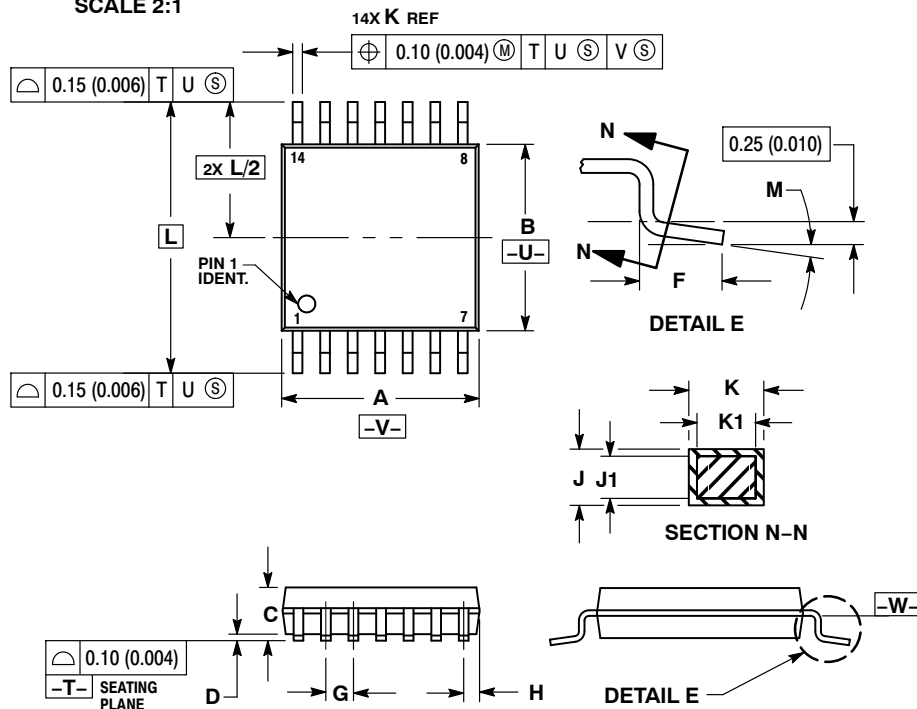
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

TSSOP-14 WB CASE 948G ISSUE C

DATE 17 FEB 2016

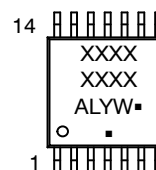


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*

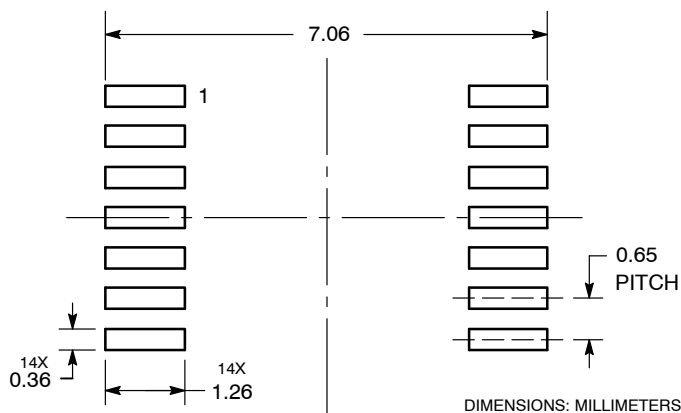


- A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT



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