

# MOSFET – Power, Dual, N-Channel, for 1-Cell Lithium-ion Battery Protection

12 V, 2.75 mΩ, 33 A

## EFC2K102ANUZ

### Overview

This Power MOSFET features a low on-state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1-cell lithium-ion battery applications.

### Features

- 2.5 V Drive
- Common-Drain type
- ESD Diode-Protected Gate
- Pb-Free, Halogen Free and RoHS Compliance

### Applications

- 1-Cell Lithium-ion Battery Charging and Discharging Switch

### Specifications

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

| Parameter                                                                  | Symbol    | Value       | Unit             |
|----------------------------------------------------------------------------|-----------|-------------|------------------|
| Source to Source Voltage                                                   | $V_{SSS}$ | 12          | V                |
| Gate to Source Voltage                                                     | $V_{GSS}$ | $\pm 8$     | V                |
| Source Current (DC)                                                        | $I_S$     | 33          | A                |
| Source Current (Pulse)<br>$PW \leq 10 \mu\text{s}$ , duty cycle $\leq 1\%$ | $I_{SP}$  | 135         | A                |
| Total Dissipation (Note 1)                                                 | $P_T$     | 3.1         | W                |
| Junction Temperature                                                       | $T_j$     | 150         | $^\circ\text{C}$ |
| Storage Temperature                                                        | $T_{stg}$ | -55 to +150 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE RATINGS

| Parameter                    | Symbol          | Value | Unit               |
|------------------------------|-----------------|-------|--------------------|
| Junction to Ambient (Note 1) | $R_{\theta JA}$ | 40.3  | $^\circ\text{C/W}$ |

1. Surface mounted on ceramic substrate ( $5000 \text{ mm}^2 \times 0.8 \text{ mm}$ ).

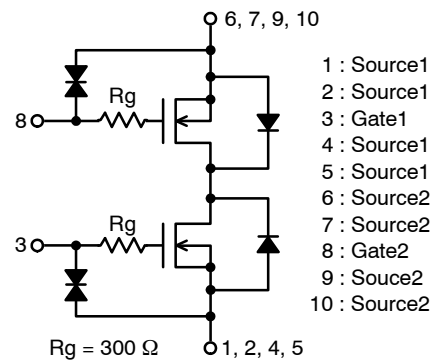


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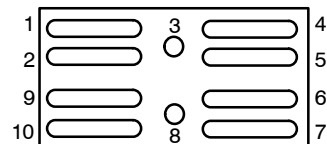
[www.onsemi.com](http://www.onsemi.com)

| $V_{SSS}$ | $R_{SS(on)}$ Max | $I_S$ Max |
|-----------|------------------|-----------|
| 12 V      | 2.75 mΩ @ 4.5 V  | 33 A      |
|           | 2.85 mΩ @ 3.8 V  |           |
|           | 3.95 mΩ @ 3.1 V  |           |
|           | 6.1 mΩ @ 2.5 V   |           |

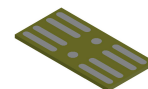
### ELECTRICAL CONNECTION N-Channel



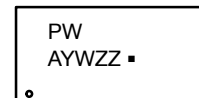
### PIN ASSIGNMENT



### MARKING DIAGRAM



WLCSP10  
2.98x1.49x0.1  
CASE 567ZG



PW = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Assembly Lot  
■ = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# EFC2K102ANUZ

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

| Parameter                                   | Symbol               | Conditions                                                                                                        | Value |      |      | Unit |
|---------------------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------|-------|------|------|------|
|                                             |                      |                                                                                                                   | Min   | Typ  | Max  |      |
| Source to Source Breakdown Voltage          | V <sub>(BR)SSS</sub> | I <sub>S</sub> = 1 mA, V <sub>GS</sub> = 0 V Test Circuit 1                                                       | 12    | –    | –    | V    |
| Zero–Gate Voltage Source Current            | I <sub>SSS</sub>     | V <sub>SS</sub> = 10 V, V <sub>GS</sub> = 0 V Test Circuit 1                                                      | –     | –    | 1    | μA   |
| Gate to Source Leakage Current              | I <sub>GSS</sub>     | V <sub>GS</sub> = ±8 V, V <sub>SS</sub> = 0 V Test Circuit 2                                                      | –     | –    | ±1   | μA   |
| Gate Threshold Voltage                      | V <sub>GS(th)</sub>  | V <sub>SS</sub> = 6 V, I <sub>S</sub> = 1 mA Test Circuit 3                                                       | 0.4   | –    | 1.3  | V    |
| Static Source to Source On–State Resistance | R <sub>SS(on)</sub>  | I <sub>S</sub> = 5 A, V <sub>GS</sub> = 4.5 V Test Circuit 4                                                      | 1.55  | 2.10 | 2.75 | mΩ   |
|                                             |                      | I <sub>S</sub> = 5 A, V <sub>GS</sub> = 3.8 V Test Circuit 4                                                      | 1.60  | 2.20 | 2.85 | mΩ   |
|                                             |                      | I <sub>S</sub> = 5 A, V <sub>GS</sub> = 3.1 V Test Circuit 4                                                      | 1.65  | 2.40 | 3.95 | mΩ   |
|                                             |                      | I <sub>S</sub> = 5 A, V <sub>GS</sub> = 2.5 V Test Circuit 4                                                      | 1.90  | 3.10 | 6.10 | mΩ   |
| Turn–ON Delay Time                          | t <sub>d(on)</sub>   | V <sub>SS</sub> = 6 V, V <sub>GS</sub> = 3.8 V, I <sub>S</sub> = 5 A,<br>R <sub>g</sub> = 10 kΩ<br>Test Circuit 5 | –     | 20   | –    | μs   |
| Rise Time                                   | t <sub>r</sub>       |                                                                                                                   | –     | 58   | –    | μs   |
| Turn–OFF Delay Time                         | t <sub>d(off)</sub>  |                                                                                                                   | –     | 115  | –    | μs   |
| Fall Time                                   | t <sub>f</sub>       |                                                                                                                   | –     | 94   | –    | μs   |
| Total Gate Charge                           | Q <sub>g</sub>       | V <sub>SS</sub> = 6 V, V <sub>GS</sub> = 3.8 V, I <sub>S</sub> = 5 A                                              | –     | 42   | –    | nC   |
| Forward Source to Source Voltage            | V <sub>F(S–S)</sub>  | I <sub>S</sub> = 3 A, V <sub>GS</sub> = 0 V<br>Test Circuit 7                                                     | –     | 0.75 | 1.20 | V    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

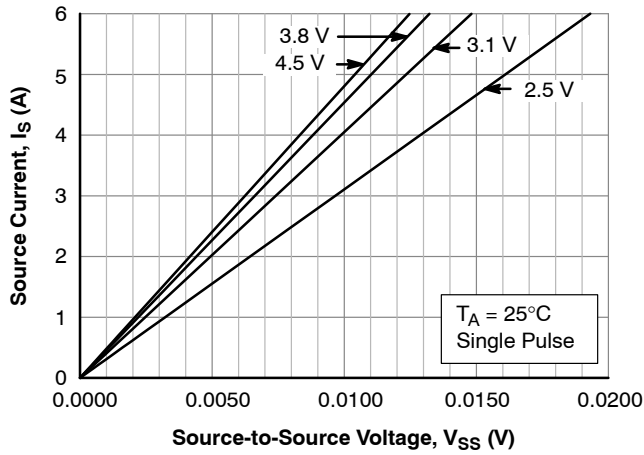


Figure 1.  $I_S - V_{SS}$

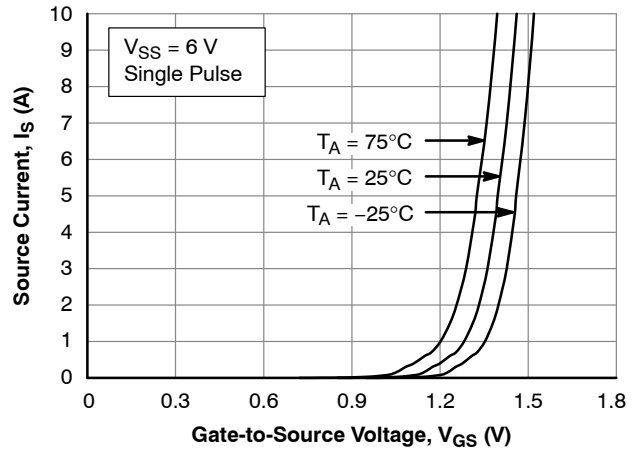


Figure 2.  $I_S - V_{GS}$

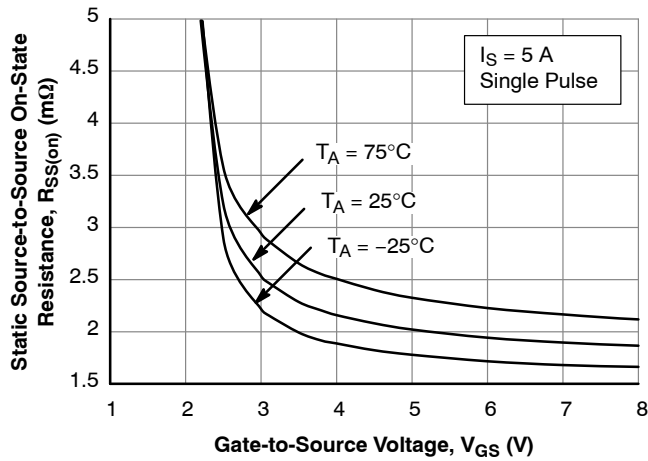


Figure 3.  $R_{SS(on)} - V_{GS}$

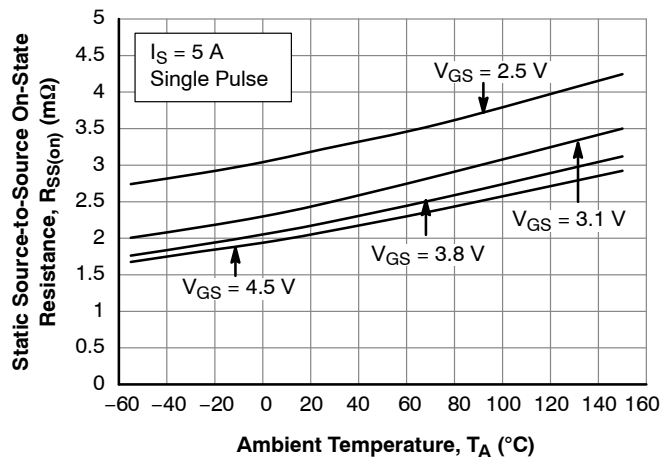


Figure 4.  $R_{SS(on)} - T_A$

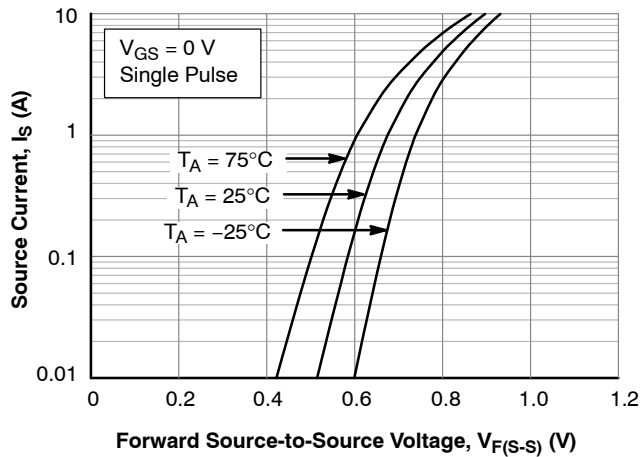


Figure 5.  $I_S - V_{F(S-S)}$

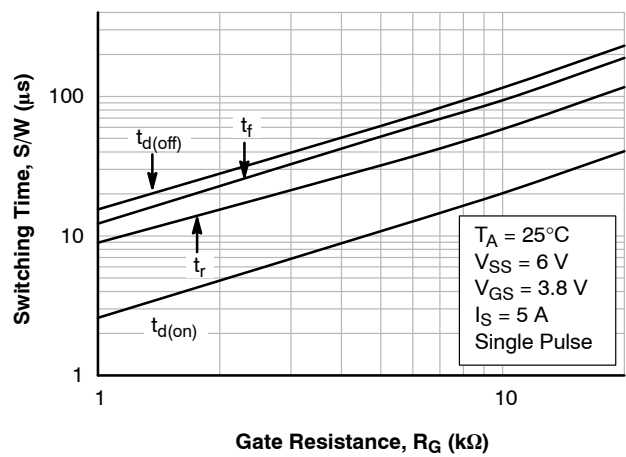


Figure 6. SW Time -  $R_G$

TYPICAL CHARACTERISTICS (Continued)

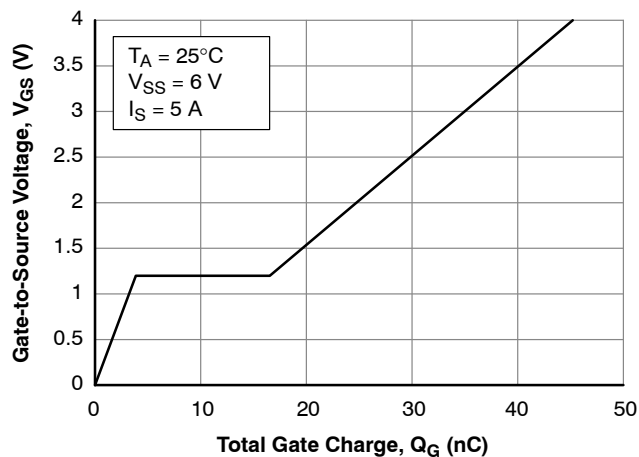


Figure 7.  $V_{GS} - Q_G$

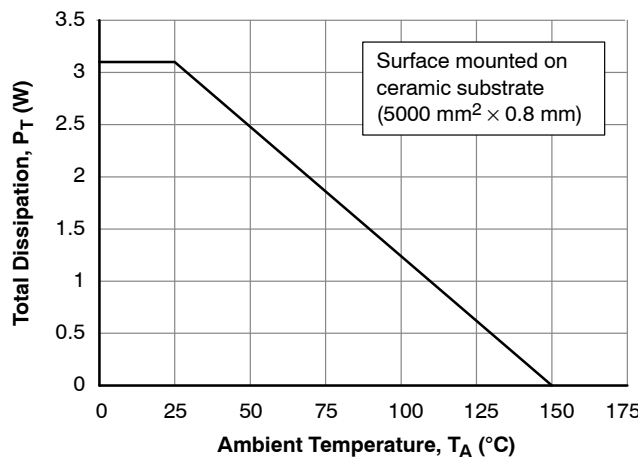


Figure 8.  $P_T - T_A$

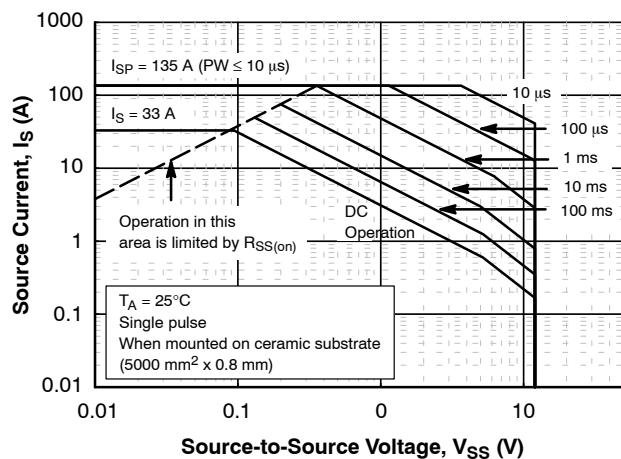


Figure 9. Safe Operating Area

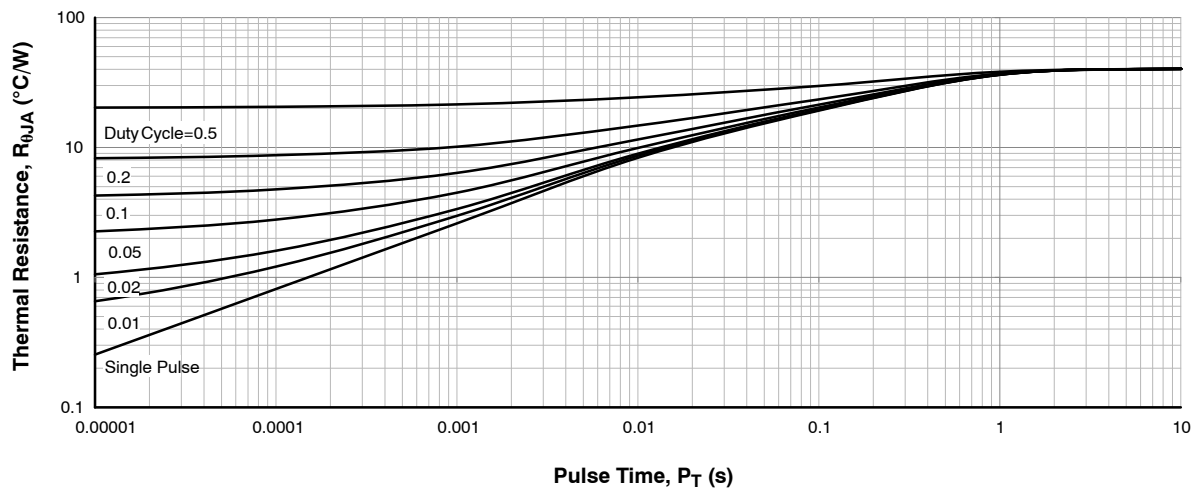
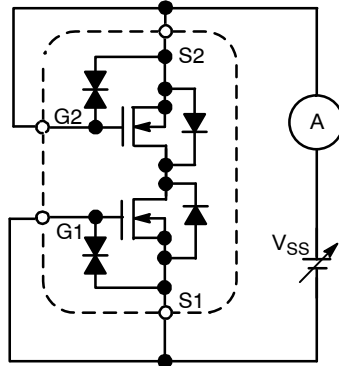


Figure 10. Thermal Response

Test Circuits are Example of Measuring FET1 Side

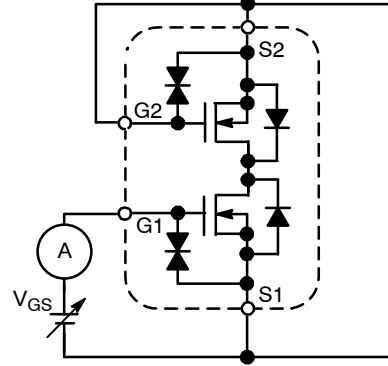
Test Circuit 1

$V_{(BR)SS} / I_{SSS}$



Test Circuit 2

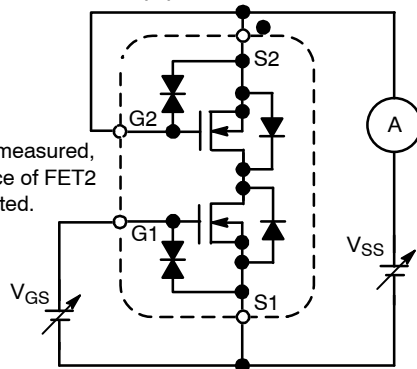
$I_{GSS}$



When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3

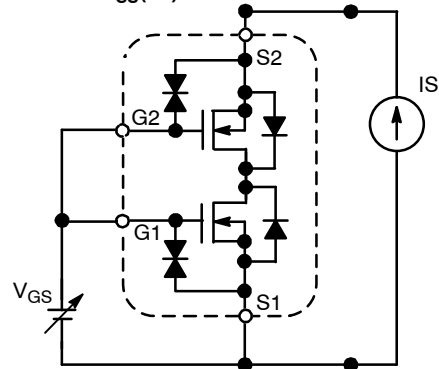
$V_{GS(th)}$



When FET1 is measured, Gate and Source of FET2 are short-circuited.

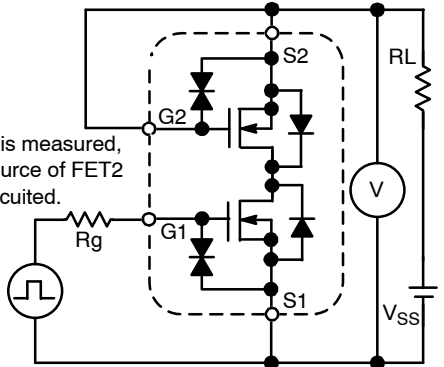
Test Circuit 4

$R_{SS(on)}$



Test Circuit 5

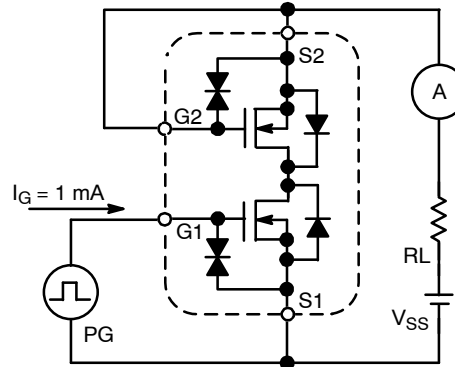
$t_d(on), t_r, t_d(off), t_f$



When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 6

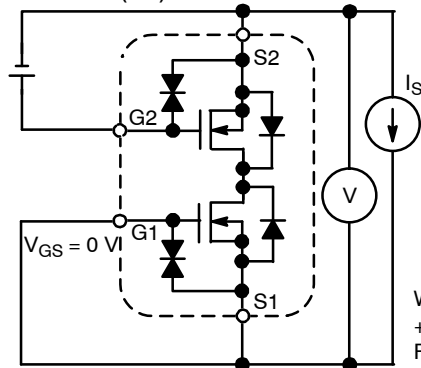
$R_g$



When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 7

$V_{F(s-s)}$



When FET1 is measured, +4.5 V is added to  $V_{GS}$  of FET2.

## EFC2K102ANUZ

### ORDERING INFORMATION

| Device          | Marking | Package                                          | Shipping (Qty / Packing) <sup>†</sup> |
|-----------------|---------|--------------------------------------------------|---------------------------------------|
| EFC2K102ANUZTDG | PW      | WLCSP10, 2.98x1.49x0.1<br>(Pb-Free/Halogen Free) | 5,000 / Tape & Reel                   |

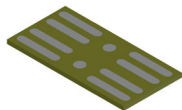
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: Since the EFC2K102ANUZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.

# MECHANICAL CASE OUTLINE

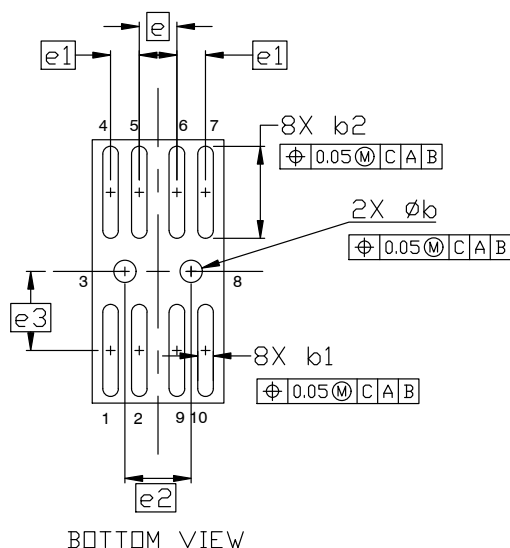
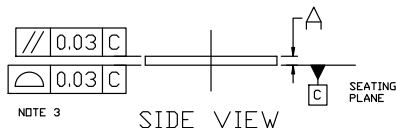
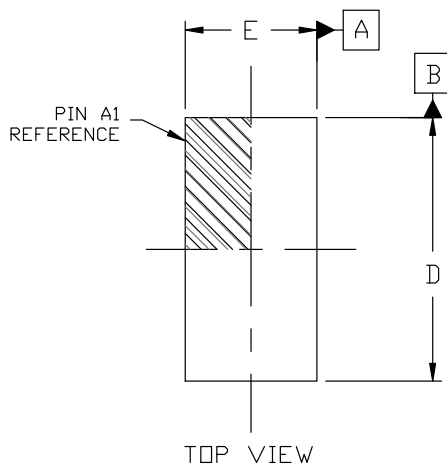
## PACKAGE DIMENSIONS

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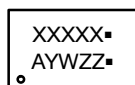


**WLCSP10 2.98x1.49x0.1**  
CASE 567ZG  
ISSUE O

DATE 27 MAY 2020



### GENERIC MARKING DIAGRAM\*



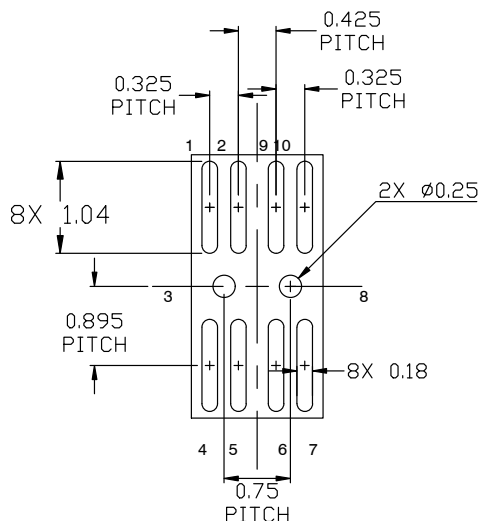
XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Assembly Lot Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO ALL PADS

| DIM | MILLIMETERS |       |       |
|-----|-------------|-------|-------|
|     | MIN.        | NDM.  | MAX.  |
| A   | 0.07        | 0.10  | 0.13  |
| b   | 0.22        | 0.25  | 0.28  |
| b1  | 0.145       | 0.175 | 0.205 |
| b2  | 1.01        | 1.04  | 1.07  |
| D   | 2.95        | 2.98  | 3.01  |
| E   | 1.46        | 1.49  | 1.52  |
| e   | 0.425 BSC   |       |       |
| e1  | 0.325 BSC   |       |       |
| e2  | 0.75 BSC    |       |       |
| e3  | 0.895 BSC   |       |       |



### RECOMMENDED MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                         |                              |                                                                                                                                                                                     |
|-------------------------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98AON21752H</b>           | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>WLCSP10 2.98x1.49x0.1</b> | <b>PAGE 1 OF 1</b>                                                                                                                                                                  |

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